

x86 Assembly Language Reference Manual

ORACLE

Part No: E36859-02
December 2014

Copyright © 1993, 2014, Oracle and/or its affiliates. All rights reserved.

This software and related documentation are provided under a license agreement containing restrictions on use and disclosure and are protected by intellectual property laws. Except as expressly permitted in your license agreement or allowed by law, you may not use, copy, reproduce, translate, broadcast, modify, license, transmit, distribute, exhibit, perform, publish, or display any part, in any form, or by any means. Reverse engineering, disassembly, or decompilation of this software, unless required by law for interoperability, is prohibited.

The information contained herein is subject to change without notice and is not warranted to be error-free. If you find any errors, please report them to us in writing.

If this is software or related documentation that is delivered to the U.S. Government or anyone licensing it on behalf of the U.S. Government, the following notice is applicable:

U.S. GOVERNMENT END USERS. Oracle programs, including any operating system, integrated software, any programs installed on the hardware, and/or documentation, delivered to U.S. Government end users are "commercial computer software" pursuant to the applicable Federal Acquisition Regulation and agency-specific supplemental regulations. As such, use, duplication, disclosure, modification, and adaptation of the programs, including any operating system, integrated software, any programs installed on the hardware, and/or documentation, shall be subject to license terms and license restrictions applicable to the programs. No other rights are granted to the U.S. Government.

This software or hardware is developed for general use in a variety of information management applications. It is not developed or intended for use in any inherently dangerous applications, including applications that may create a risk of personal injury. If you use this software or hardware in dangerous applications, then you shall be responsible to take all appropriate fail-safe, backup, redundancy, and other measures to ensure its safe use. Oracle Corporation and its affiliates disclaim any liability for any damages caused by use of this software or hardware in dangerous applications.

Oracle and Java are registered trademarks of Oracle and/or its affiliates. Other names may be trademarks of their respective owners.

Intel and Intel Xeon are trademarks or registered trademarks of Intel Corporation. All SPARC trademarks are used under license and are trademarks or registered trademarks of SPARC International, Inc. AMD, Opteron, the AMD logo, and the AMD Opteron logo are trademarks or registered trademarks of Advanced Micro Devices. UNIX is a registered trademark of The Open Group.

This software or hardware and documentation may provide access to or information on content, products, and services from third parties. Oracle Corporation and its affiliates are not responsible for and expressly disclaim all warranties of any kind with respect to third-party content, products, and services. Oracle Corporation and its affiliates will not be responsible for any loss, costs, or damages incurred due to your access to or use of third-party content, products, or services.

Copyright © 1993, 2014, Oracle et/ou ses affiliés. Tous droits réservés.

Ce logiciel et la documentation qui l'accompagne sont protégés par les lois sur la propriété intellectuelle. Ils sont concédés sous licence et soumis à des restrictions d'utilisation et de divulgation. Sauf disposition de votre contrat de licence ou de la loi, vous ne pouvez pas copier, reproduire, traduire, diffuser, modifier, breveter, transmettre, distribuer, exposer, exécuter, publier ou afficher le logiciel, même partiellement, sous quelque forme et par quelque procédé que ce soit. Par ailleurs, il est interdit de procéder à toute ingénierie inverse du logiciel, de le désassembler ou de le décompiler, excepté à des fins d'interopérabilité avec des logiciels tiers ou tel que prescrit par la loi.

Les informations fournies dans ce document sont susceptibles de modification sans préavis. Par ailleurs, Oracle Corporation ne garantit pas qu'elles soient exemptes d'erreurs et vous invite, le cas échéant, à lui en faire part par écrit.

Si ce logiciel, ou la documentation qui l'accompagne, est concédé sous licence au Gouvernement des Etats-Unis, ou à toute entité qui délivre la licence de ce logiciel ou l'utilise pour le compte du Gouvernement des Etats-Unis, la notice suivante s'applique:

U.S. GOVERNMENT END USERS. Oracle programs, including any operating system, integrated software, any programs installed on the hardware, and/or documentation, delivered to U.S. Government end users are "commercial computer software" pursuant to the applicable Federal Acquisition Regulation and agency-specific supplemental regulations. As such, use, duplication, disclosure, modification, and adaptation of the programs, including any operating system, integrated software, any programs installed on the hardware, and/or documentation, shall be subject to license terms and license restrictions applicable to the programs. No other rights are granted to the U.S. Government.

Ce logiciel ou matériel a été développé pour un usage général dans le cadre d'applications de gestion des informations. Ce logiciel ou matériel n'est pas conçu ni n'est destiné à être utilisé dans des applications à risque, notamment dans des applications pouvant causer des dommages corporels. Si vous utilisez ce logiciel ou matériel dans le cadre d'applications dangereuses, il est de votre responsabilité de prendre toutes les mesures de secours, de sauvegarde, de redondance et autres mesures nécessaires à son utilisation dans des conditions optimales de sécurité. Oracle Corporation et ses affiliés déclinent toute responsabilité quant aux dommages causés par l'utilisation de ce logiciel ou matériel pour ce type d'applications.

Oracle et Java sont des marques déposées d'Oracle Corporation et/ou de ses affiliés. Tout autre nom mentionné peut correspondre à des marques appartenant à d'autres propriétaires qu'Oracle.

Intel et Intel Xeon sont des marques ou des marques déposées d'Intel Corporation. Toutes les marques SPARC sont utilisées sous licence et sont des marques ou des marques déposées de SPARC International, Inc. AMD, Opteron, le logo AMD et le logo AMD Opteron sont des marques ou des marques déposées d'Advanced Micro Devices. UNIX est une marque déposée d'The Open Group.

Ce logiciel ou matériel et la documentation qui l'accompagne peuvent fournir des informations ou des liens donnant accès à des contenus, des produits et des services émanant de tiers. Oracle Corporation et ses affiliés déclinent toute responsabilité ou garantie expresse quant aux contenus, produits ou services émanant de tiers. En aucun cas, Oracle Corporation et ses affiliés ne sauraient être tenus pour responsables des pertes subies, des coûts occasionnés ou des dommages causés par l'accès à des contenus, produits ou services tiers, ou à leur utilisation.

Contents

Using This Documentation	9
1 Overview of the Oracle Solaris x86 Assembler	11
1.1 Assembler Overview	11
1.2 Syntax Differences Between x86 Assemblers	11
2 Oracle Solaris x86 Assembly Language Syntax	13
2.1 Lexical Conventions	13
2.1.1 Statements	13
2.1.2 Tokens	15
2.2 Instructions, Operands, and Addressing	17
2.2.1 Instructions	17
2.2.2 Operands	18
2.3 Assembler Directives	20
3 Instruction Set Mapping	27
3.1 Instruction Overview	28
3.2 General-Purpose Instructions	29
3.2.1 Data Transfer Instructions	29
3.2.2 Binary Arithmetic Instructions	33
3.2.3 Decimal Arithmetic Instructions	33
3.2.4 Logical Instructions	34
3.2.5 Shift and Rotate Instructions	34
3.2.6 Bit and Byte Instructions	35
3.2.7 Control Transfer Instructions	36
3.2.8 String Instructions	38
3.2.9 I/O Instructions	40
3.2.10 Flag Control (EFLAG) Instructions	40
3.2.11 Segment Register Instructions	41
3.2.12 Miscellaneous Instructions	42

3.3	Floating-Point Instructions	42
3.3.1	Data Transfer Instructions (Floating Point)	42
3.3.2	Basic Arithmetic Instructions (Floating-Point)	43
3.3.3	Comparison Instructions (Floating-Point)	44
3.3.4	Transcendental Instructions (Floating-Point)	45
3.3.5	Load Constants (Floating-Point) Instructions	46
3.3.6	Control Instructions (Floating-Point)	46
3.4	SIMD State Management Instructions	48
3.5	AES Instructions	48
3.5.1	Advanced Vector Extensions of AES Instructions	49
3.6	AVX Instructions	49
3.7	AVX2 Instructions	74
3.8	BMI1 Instructions	82
3.9	BMI2 Instructions	82
3.10	F16C Instructions	83
3.11	FMA Instructions	83
3.12	FSGSBASE Instructions	90
3.13	MMX Instructions	90
3.13.1	Data Transfer Instructions (MMX)	90
3.13.2	Conversion Instructions (MMX)	91
3.13.3	Packed Arithmetic Instructions (MMX)	91
3.13.4	Comparison Instructions (MMX)	93
3.13.5	Logical Instructions (MMX)	93
3.13.6	Shift and Rotate Instructions (MMX)	94
3.13.7	State Management Instructions (MMX)	94
3.14	MOVBE Instructions	95
3.15	PCLMULQDQ Instructions	95
3.16	RDRAND Instructions	95
3.17	SSE Instructions	95
3.17.1	SIMD Single-Precision Floating-Point Instructions (SSE)	96
3.17.2	MXCSR State Management Instructions (SSE)	101
3.17.3	64–Bit SIMD Integer Instructions (SSE)	101
3.17.4	Miscellaneous Instructions (SSE)	102
3.18	SSE2 Instructions	103
3.18.1	SSE2 Packed and Scalar Double-Precision Floating-Point Instructions	103
3.18.2	SSE2 Packed Single-Precision Floating-Point Instructions	108
3.18.3	SSE2 128–Bit SIMD Integer Instructions	109
3.18.4	SSE2 Miscellaneous Instructions	110
3.19	SSE3 Instructions	111

3.20 SSE4a Instructions	112
3.21 SSE4.1 Instructions	112
3.22 SSE4.2 Instructions	115
3.23 SSSE3 Instructions	115
3.24 Transactional Synchronization Extensions	116
3.25 Operating System Support Instructions	117
3.26 VMX Instructions	118
3.27 XSAVE Instructions	119
3.28 3DNow Instructions	119
3.29 3DNowx Instructions	121
3.30 64–Bit AMD Opteron Considerations	121
A Using the Assembler Command Line	123
A.1 Assembler Command Line	123
A.2 Assembler Command Line Options	123
A.3 Disassembling Object Code	127
Index	129

Tables

TABLE 3-1	Instruction References	28
TABLE 3-2	Data Transfer Instructions	29
TABLE 3-3	Binary Arithmetic Instructions	33
TABLE 3-4	Decimal Arithmetic Instructions	33
TABLE 3-5	Logical Instructions	34
TABLE 3-6	Shift and Rotate Instructions	34
TABLE 3-7	Bit and Byte Instructions	35
TABLE 3-8	Control Transfer Instructions	37
TABLE 3-9	String Instructions	39
TABLE 3-10	I/O Instructions	40
TABLE 3-11	Flag Control Instructions	41
TABLE 3-12	Segment Register Instructions	41
TABLE 3-13	Miscellaneous Instructions	42
TABLE 3-14	Data Transfer Instructions (Floating-Point)	42
TABLE 3-15	Basic Arithmetic Instructions (Floating-Point)	43
TABLE 3-16	Comparison Instructions (Floating-Point)	45
TABLE 3-17	Transcendental Instructions (Floating-Point)	45
TABLE 3-18	Load Constants Instructions (Floating-Point)	46
TABLE 3-19	Control Instructions (Floating-Point)	46
TABLE 3-20	SIMD State Management Instructions	48
TABLE 3-21	AES Instructions	48
TABLE 3-22	Advanced Vector Extensions of AES Instructions	49
TABLE 3-23	AVX Instructions	49
TABLE 3-24	AVX2 Instructions	74
TABLE 3-25	BMI1 Instructions	82
TABLE 3-26	BMI2 Instructions	82
TABLE 3-27	F16C Instructions	83
TABLE 3-28	FMA Instructions	83
TABLE 3-29	FSGSBASE Instructions	90
TABLE 3-30	Data Transfer Instructions (MMX)	91

TABLE 3-31	Conversion Instructions (MMX)	91
TABLE 3-32	Packed Arithmetic Instructions (MMX)	92
TABLE 3-33	Comparison Instructions (MMX)	93
TABLE 3-34	Logical Instructions (MMX)	93
TABLE 3-35	Shift and Rotate Instructions (MMX)	94
TABLE 3-36	State Management Instructions (MMX)	94
TABLE 3-37	MOVBE Instructions	95
TABLE 3-38	PCLMULQDQ Instructions	95
TABLE 3-39	RDRAND Instructions	95
TABLE 3-40	Data Transfer Instructions (SSE)	96
TABLE 3-41	Packed Arithmetic Instructions (SSE)	97
TABLE 3-42	Comparison Instructions (SSE)	99
TABLE 3-43	Logical Instructions (SSE)	99
TABLE 3-44	Shuffle and Unpack Instructions (SSE)	100
TABLE 3-45	Conversion Instructions (SSE)	100
TABLE 3-46	MXCSR State Management Instructions (SSE)	101
TABLE 3-47	64-Bit SIMD Integer Instructions (SSE)	101
TABLE 3-48	Miscellaneous Instructions (SSE)	102
TABLE 3-49	SSE2 Data Movement Instructions	103
TABLE 3-50	SSE2 Packed Arithmetic Instructions	104
TABLE 3-51	SSE2 Logical Instructions	105
TABLE 3-52	SSE2 Compare Instructions	106
TABLE 3-53	SSE2 Shuffle and Unpack Instructions	107
TABLE 3-54	SSE2 Conversion Instructions	107
TABLE 3-55	SSE2 Packed Single-Precision Floating-Point Instructions	109
TABLE 3-56	SSE2 128-Bit SIMD Integer Instructions	109
TABLE 3-57	SSE2 Miscellaneous Instructions	110
TABLE 3-58	SSE3 Instructions	111
TABLE 3-59	SSE4a Instructions	112
TABLE 3-60	SSE4.1 Instructions	112
TABLE 3-61	SSE4.2 Instructions	115
TABLE 3-62	SSSE3 Instructions	115
TABLE 3-63	HLE Instructions	116
TABLE 3-64	RTM Instructions	116
TABLE 3-65	Operating System Support Instructions	117
TABLE 3-66	VMX Instructions	118
TABLE 3-67	XSAVE Instructions	119
TABLE 3-68	3DNow Instructions	119
TABLE 3-69	3DNowx Instructions	121

Using This Documentation

- **Overview** – The *Oracle Solaris x86 Assembly Language Reference Manual* documents the syntax of the Oracle Solaris x86 assembly language. This manual is provided to help experienced programmers understand the assembly language output of Oracle Solaris compilers. This manual is neither an introductory book about assembly language programming nor a reference manual for the x86 architecture.
- **Audience** – This manual is intended for experienced x86 assembly language programmers who are familiar with the x86 architecture.
- **Required knowledge** – You should have a thorough knowledge of assembly language programming in general and be familiar with the x86 architecture in specific. You should be familiar with the ELF object file format. This manual assumes that you have the following documentation available for reference:
 - [Intel 64 and IA-32 Architectures Software Developer Manuals](#).
 - *AMD64 Architecture Programmer's Manual* (Advanced Micro Devices, 2003). Volume 1: *Application Programming*. Volume 2: *System Programming*. Volume 3: *General-Purpose and System Instructions*. Volume 4: *128-Bit Media Instructions*. Volume 5: *64-Bit Media and x87 Floating-Point Instructions*.
 - “Oracle Solaris 11.2 Linkers and Libraries Guide ”
 - [Oracle Solaris Studio 12.3: C User's Guide](#)
 - Man pages for the [as\(1\)](#), [ld\(1\)](#), and [dis\(1\)](#) utilities.

How This Book Is Organized

[Chapter 1, “Overview of the Oracle Solaris x86 Assembler”](#) provides an overview of the x86 functionality supported by the Oracle Solaris x86 assembler.

[Chapter 2, “Oracle Solaris x86 Assembly Language Syntax”](#) documents the syntax of the Solaris x86 assembly language.

[Chapter 3, “Instruction Set Mapping”](#) maps Oracle Solaris x86 assembly language instruction mnemonics to the native x86 instruction set.

Product Documentation Library

Late-breaking information and known issues for this product are included in the documentation library at <http://www.oracle.com/pls/topic/lookup?ctx=E36784>.

Access to Oracle Support

Oracle customers have access to electronic support through My Oracle Support. For information, visit <http://www.oracle.com/pls/topic/lookup?ctx=acc&id=info> or visit <http://www.oracle.com/pls/topic/lookup?ctx=acc&id=trs> if you are hearing impaired.

Feedback

Provide feedback about this documentation at <http://www.oracle.com/goto/docfeedback>.

Overview of the Oracle Solaris x86 Assembler

This chapter provides a brief overview of the Oracle Solaris x86 assembler as. This chapter discusses the following topics:

- [“1.1 Assembler Overview” on page 11](#)
- [“1.2 Syntax Differences Between x86 Assemblers” on page 11](#)

1.1 Assembler Overview

The Oracle Solaris x86 assembler as translates Oracle Solaris x86 assembly language into Executable and Linking Format (ELF) relocatable object files that can be linked with other object files to create an executable file or a shared object file. (See [Chapter 12, “Object File Format,”](#) in [“Oracle Solaris 11.2 Linkers and Libraries Guide”](#) for a complete discussion of ELF object file format.) The assembler supports macro processing by the C preprocessor (cpp) or the m4 macro processor.

1.2 Syntax Differences Between x86 Assemblers

There is no standard assembly language for the x86 architecture. Vendor implementations of assemblers for the x86 architecture instruction sets differ in syntax and functionality. The syntax of the Oracle Solaris x86 assembler is compatible with the syntax of the assembler distributed with earlier releases of the UNIX operating system (this syntax is sometimes termed “AT&T syntax”). Developers familiar with other assemblers derived from the original UNIX assemblers, such as the Free Software Foundation's `gas`, will find the syntax of the Oracle Solaris x86 assembler very straightforward.

However, the syntax of x86 assemblers distributed by Intel and Microsoft (sometimes termed “Intel syntax”) differs significantly from the syntax of the Oracle Solaris x86 assembler. These differences are most pronounced in the handling of instruction operands:

- The Oracle Solaris and Intel assemblers use the opposite order for source and destination operands.

- The Oracle Solaris assembler specifies the size of memory operands by adding a suffix to the instruction mnemonic, while the Intel assembler prefixes the memory operands.
- The Oracle Solaris assembler prefixes immediate operands with a dollar sign (\$) (ASCII 0x24), while the Intel assembler does not delimit immediate operands.

See [Chapter 2, “Oracle Solaris x86 Assembly Language Syntax”](#) for additional differences between x86 assemblers.

Oracle Solaris x86 Assembly Language Syntax

This chapter documents the syntax of the Oracle Solaris x86 assembly language.

- [“2.1 Lexical Conventions” on page 13](#)
- [“2.2 Instructions, Operands, and Addressing” on page 17](#)
- [“2.3 Assembler Directives” on page 20](#)

2.1 Lexical Conventions

This section discusses the lexical conventions of the Oracle Solaris x86 assembly language.

2.1.1 Statements

An x86 assembly language program consists of one or more files containing *statements*. A *statement* consists of *tokens* separated by *whitespace* and terminated by either a newline character (ASCII 0x0A) or a semicolon (;) (ASCII 0x3B). *Whitespace* consists of spaces (ASCII 0x20), tabs (ASCII 0x09), and form feeds (ASCII 0x0B) that are not contained in a string or comment. More than one statement can be placed on a single input line provided that each statement is terminated by a semicolon. A statement can consist of a *comment*. *Empty statements*, consisting only of whitespace, are allowed.

2.1.1.1 Comments

A *comment* can be appended to a statement. The comment consists of the slash character (/) (ASCII 0x2F) followed by the text of the comment. The comment is terminated by the newline that terminates the statement.

2.1.1.2 Labels

A *label* can be placed at the beginning of a statement. During assembly, the label is assigned the current value of the active location counter and serves as an instruction operand. There are two types of labels: *symbolic* and *numeric*.

Symbolic Labels

A *symbolic* label consists of an *identifier* (or *symbol*) followed by a colon (:) (ASCII 0x3A). Symbolic labels must be defined only once. Symbolic labels have *global* scope and appear in the object file's symbol table.

Symbolic labels with identifiers beginning with a period (.) (ASCII 0x2E) are considered to have *local* scope and are not included in the object file's symbol table.

Numeric Labels

A *numeric* label consists of a unsigned decimal *int32* value followed by a colon (:). Numeric labels are used only for local reference and are not included in the object file's symbol table. Numeric labels have limited scope and can be redefined repeatedly.

When a numeric label is used as a reference (as an instruction operand, for example), the suffixes *b* (“backward”) or *f* (“forward”) should be added to the numeric label. For numeric label *N*, the reference *Nb* refers to the nearest label *N* defined *before* the reference, and the reference *Nf* refers to the nearest label *N* defined *after* the reference. The following example illustrates the use of numeric labels:

```
1:          / define numeric label "1"
one:       / define symbolic label "one"

/ ... assembler code ...

jmp 1f     / jump to first numeric label "1" defined
          / after this instruction
          / (this reference is equivalent to label "two")

jmp 1b     / jump to last numeric label "1" defined
          / before this instruction
          / (this reference is equivalent to label "one")

1:          / redefine label "1"
two:       / define symbolic label "two"

jmp 1b     / jump to last numeric label "1" defined
          / before this instruction
          / (this reference is equivalent to label "two")
```

2.1.2 Tokens

There are five classes of tokens:

- Identifiers (symbols)
- Keywords
- Numerical constants
- String Constants
- Operators

2.1.2.1 Identifiers

An *identifier* is an arbitrarily-long sequence of letters and digits. The first character must be a letter; the underscore (`_`) (ASCII 0x5F) and the period (`.`) (ASCII 0x2E) are considered to be letters. Case is significant: uppercase and lowercase letters are different.

2.1.2.2 Keywords

Keywords such as x86 instruction mnemonics (“opcodes”) and assembler directives are reserved for the assembler and should not be used as identifiers. See [Chapter 3, “Instruction Set Mapping”](#) for a list of the Oracle Solaris x86 mnemonics. See [“2.3 Assembler Directives” on page 20](#) for the list of as assembler directives.

2.1.2.3 Numerical Constants

Numbers in the x86 architecture can be *integers* or *floating point*. Integers can be *signed* or *unsigned*, with signed integers represented in two's complement representation. Floating-point numbers can be: single-precision floating-point; double-precision floating-point; and double-extended precision floating-point.

Integer Constants

Integers can be expressed in several bases:

- **Decimal.** Decimal integers begin with a non-zero digit followed by zero or more decimal digits (0–9).
- **Binary.** Binary integers begin with “0b” or “0B” followed by zero or more binary digits (0, 1).
- **Octal.** Octal integers begin with zero (0) followed by zero or more octal digits (0–7).

- **Hexadecimal.** Hexadecimal integers begin with “0x” or “0X” followed by one or more hexadecimal digits (0–9, A–F). Hexadecimal digits can be either uppercase or lowercase.

Floating Point Constants

Floating point constants have the following format:

- **Sign** (optional) – either plus (+) or minus (–)
- **Integer** (optional) – zero or more decimal digits (0–9)
- **Fraction** (optional) – decimal point (.) followed by zero or more decimal digits
- **Exponent** (optional) – the letter “e” or “E”, followed by an optional sign (plus or minus), followed by one or more decimal digits (0–9)

A valid floating point constant must have either an integer part or a fractional part.

2.1.2.4 String Constants

A *string* constant consists of a sequence of characters enclosed in double quotes (") (ASCII 0x22). To include a double-quote character ("), single-quote character ('), or backslash character (\) within a string, precede the character with a backslash (\) (ASCII 0x5C). A character can be expressed in a string as its ASCII value in octal preceded by a backslash (for example, the letter “J” could be expressed as “\112”). The assembler accepts the following escape sequences in strings:

Escape Sequence	Character Name	ASCII Value (hex)
\n	newline	0A
\r	carriage return	0D
\b	backspace	08
\t	horizontal tab	09
\f	form feed	0C
\v	vertical tab	0B

2.1.2.5 Operators

The assembler supports the following operators for use in expressions. Operators have no assigned precedence. Expressions can be grouped in square brackets ([]) to establish precedence.

+	Addition
-	Subtraction
*	Multiplication
\/	Division
&	Bitwise logical AND
	Bitwise logical OR
>>	Shift right
<<	Shift left
\%	Remainder
!	Bitwise logical AND NOT
^	Bitwise logical XOR

Note - The asterisk (*), slash (/), and percent sign (%) characters are overloaded. When used as operators in an expression, these characters must be preceded by the backslash character (\).

2.2 Instructions, Operands, and Addressing

Instructions are operations performed by the CPU. *Operands* are entities operated upon by the instruction. *Addresses* are the locations in memory of specified data.

2.2.1 Instructions

An *instruction* is a statement that is executed at runtime. An x86 instruction statement can consist of four parts:

- Label (optional)
- Instruction (required)
- Operands (instruction specific)
- Comment (optional)

See [“2.1.1 Statements” on page 13](#) for the description of labels and comments.

The terms *instruction* and *mnemonic* are used interchangeably in this document to refer to the names of x86 instructions. Although the term *opcode* is sometimes used as a synonym for *instruction*, this document reserves the term *opcode* for the hexadecimal representation of the instruction value.

For most instructions, the Oracle Solaris x86 assembler mnemonics are the same as the Intel or AMD mnemonics. However, the Oracle Solaris x86 mnemonics might appear to be different because the Oracle Solaris mnemonics are suffixed with a one-character modifier that specifies the size of the instruction operands. That is, the Oracle Solaris assembler derives its operand type information from the instruction name and the suffix. If a mnemonic is specified with no type suffix, the operand type defaults to long. Possible operand types and their instruction suffixes are:

b	Byte (8-bit)
w	Word (16-bit)
l	Long (32-bit) (default)
q	Quadword (64-bit)

The assembler recognizes the following suffixes for x87 floating-point instructions:

[no suffix]	Instruction operands are registers only
l (“long”)	Instruction operands are 64-bit
s (“short”)	Instruction operands are 32-bit

See [Chapter 3, “Instruction Set Mapping”](#) for a mapping between Oracle Solaris x86 assembly language mnemonics and the equivalent Intel or AMD mnemonics.

2.2.2 Operands

An x86 instruction can have zero to three operands. Operands are separated by commas (,) (ASCII 0x2C). For instructions with two operands, the first (lefthand) operand is the *source* operand, and the second (righthand) operand is the *destination* operand (that is, *source* → *destination*).

Note - The Intel assembler uses the opposite order (*destination* ← *source*) for operands.

Operands can be *immediate* (that is, constant expressions that evaluate to an inline value), *register* (a value in the processor number registers), or *memory* (a value stored in memory).

An *indirect* operand contains the address of the actual operand value. Indirect operands are specified by prefixing the operand with an asterisk (*) (ASCII 0x2A). Only jump and call instructions can use indirect operands.

- *Immediate* operands are prefixed with a dollar sign (\$) (ASCII 0x24)
- *Register* names are prefixed with a percent sign (%) (ASCII 0x25)
- *Memory* operands are specified either by the name of a variable or by a register that contains the address of a variable. A variable name implies the address of a variable and instructs the computer to reference the contents of memory at that address. Memory references have the following syntax:
segment:offset(base, index, scale).
 - *Segment* is any of the x86 architecture segment registers. *Segment* is optional: if specified, it must be separated from *offset* by a colon (:). If *segment* is omitted, the value of %ds (the default segment register) is assumed.
 - *Offset* is the displacement from *segment* of the desired memory value. *Offset* is optional.
 - *Base* and *index* can be any of the general 32-bit number registers.
 - *Scale* is a factor by which *index* is to be multiplied before being added to *base* to specify the address of the operand. *Scale* can have the value of 1, 2, 4, or 8. If *scale* is not specified, the default value is 1.

Some examples of memory addresses are:

<code>movl var, %eax</code>	Move the contents of memory location <code>var</code> into number register <code>%eax</code> .
<code>movl %cs:var, %eax</code>	Move the contents of memory location <code>var</code> in the code segment (register <code>%cs</code>) into number register <code>%eax</code> .
<code>movl \$var, %eax</code>	Move the address of <code>var</code> into number register <code>%eax</code> .
<code>movl array_base(%esi), %eax</code>	Add the address of memory location <code>array_base</code> to the contents of number register <code>%esi</code> to determine an address in memory. Move the contents of this address into number register <code>%eax</code> .
<code>movl (%ebx, %esi, 4), %eax</code>	Multiply the contents of number register <code>%esi</code> by 4 and add the result to the contents of number register <code>%ebx</code> to produce a memory reference. Move the contents of this memory location into number register <code>%eax</code> .
<code>movl struct_base(%ebx, %esi, 4), %eax</code>	Multiply the contents of number register <code>%esi</code> by 4, add the result to the contents of number register <code>%ebx</code> , and add the result to the address of <code>struct_base</code> to produce an address. Move the contents of this address into number register <code>%eax</code> .

2.3 Assembler Directives

Directives are commands that are part of the assembler syntax but are not related to the x86 processor instruction set. All assembler directives begin with a period (.) (ASCII 0x2E).

<code>.align <i>integer</i>, <i>pad</i></code>	The <code>.align</code> directive causes the next data generated to be aligned modulo <i>integer</i> bytes. <i>Integer</i> must be a positive integer expression and must be a power of 2. If specified, <i>pad</i> is an integer byte value used for padding. The default value of <i>pad</i> for the <code>.text</code> section is 0x90 (nop); for other sections, the default value of <i>pad</i> is zero (0).
<code>.ascii "<i>string</i>"</code>	The <code>.ascii</code> directive places the characters in <i>string</i> into the object module at the current location but does <i>not</i> terminate the string with a null byte (0). <i>String</i> must be enclosed in double quotes (") (ASCII 0x22). The <code>.ascii</code> directive is not valid for the <code>.bss</code> section.
<code>.bcd <i>integer</i></code>	The <code>.bcd</code> directive generates a packed decimal (80-bit) value into the current section. The <code>.bcd</code> directive is not valid for the <code>.bss</code> section.
<code>.bss</code>	The <code>.bss</code> directive changes the current section to <code>.bss</code> .
<code>.bss <i>symbol</i>, <i>integer</i></code>	Define <i>symbol</i> in the <code>.bss</code> section and add <i>integer</i> bytes to the value of the location counter for <code>.bss</code> . When issued with arguments, the <code>.bss</code> directive does not change the current section to <code>.bss</code> . <i>Integer</i> must be positive.
<code>.byte <i>byte1</i>, <i>byte2</i>, ..., <i>byteN</i></code>	The <code>.byte</code> directive generates initialized bytes into the current section. The <code>.byte</code> directive is not valid for the <code>.bss</code> section. Each <i>byte</i> must be an 8-bit value.
<code>.2byte <i>expression1</i>, <i>expression2</i>, ..., <i>expressionN</i></code>	Refer to the description of the <code>.value</code> directive.
<code>.4byte <i>expression1</i>, <i>expression2</i>, ..., <i>expressionN</i></code>	Refer to the description of the <code>.long</code> directive.
<code>.8byte <i>expression1</i>, <i>expression2</i>, ..., <i>expressionN</i></code>	Refer to the description of the <code>.quad</code> directive.

<code>.cfi_adjust_cfa_offset OFFSET</code>	The <code>.cfi_adjust_cfa_offset</code> directive is similar to <code>.cfi_def_cfa_offset</code> directive but <code>OFFSET</code> is a relative value that is added or subtracted from the previous offset.
<code>.cfi_def_cfa_offset OFFSET</code>	The <code>.cfi_def_cfa_offset</code> directive, modifies the rule for computing CFA. The value of the register remains the same, but <code>OFFSET</code> is new. Note that this is the absolute offset that will be added to a defined register to compute the CFA address.
<code>.cfi_def_cfa REGISTER, OFFSET</code>	The <code>.cfi_def_cfa</code> directive, defines a rule to compute CFA. This directive takes address from <code>REGISTER</code> and adds <code>OFFSET</code> to it.
<code>.cfi_def_cfa_register REGISTER</code>	The <code>.cfi_def_cfa_register</code> directive, modifies the rule for computing CFA. The register in the CFA is set to a new value. The offset remains the same.
<code>.cfi_endproc</code>	The <code>.cfi_endproc</code> directive, is used at the end of a function where it closes its unwind entry previously opened by <code>.cfi_startproc</code> and emits it to <code>.eh_frame</code> .
<code>.cfi_escape EXPRESSION[, ...]</code>	The <code>.cfi_escape</code> directive, allows you to add arbitrary bytes to the unwind information. You can use this directive to add OS-specific CFI opcodes, or generic CFI opcodes that the assembler does not support.
<code>.cfi_ksda encoding [, exp]</code>	The <code>.cfi_ksda</code> directive, defines KSDA and its encoding. The <i>encoding</i> should be a constant which determines how the KSDA should be encoded. If the value of <i>encoding</i> is 255 (<code>DW_EH_PE_omit</code>), second argument is not present, otherwise second argument should be a constant or a symbol name. The default directive used after <code>.cfi_startproc</code> directive is <code>.cfi_ksda 0xff</code> .
<code>.cfi_offset REGISTER, OFFSET</code>	The <code>.cfi_offset</code> directive, saves the previous value of <code>REGISTER</code> at offset <code>OFFSET</code> from CFA.
<code>.cfi_personality encoding [, exp]</code>	The <code>.cfi_personality</code> directive, defines the personality routine and its encoding. The <i>encoding</i> must be a constant which determines how the personality should be encoded. If the value of <i>encoding</i> is 255 (<code>DW_EH_PE_omit</code>), second argument is not present, otherwise second argument should be a constant or a symbol name. When you are using indirect encodings, the symbol provided should be the location where personality can be loaded from and not the personality routine itself. The default directive used after <code>.cfi_startproc</code> directive is <code>.cfi_personality 0xff</code> .

<code>.cfi_register REGISTER1 REGISTER2</code>	The <code>.cfi_register REGISTER1 REGISTER2</code> directive, saves the previous value of <code>REGISTER1</code> in register <code>REGISTER2</code> .
<code>.cfi_rel_offset REGISTER, OFFSET</code>	In the <code>.cfi_rel_offset</code> directive, saves the previous value of <code>REGISTER</code> at offset <code>OFFSET</code> from the current CFA register. This is transformed to <code>.cfi_offset</code> using the known displacement of the CFA register from the CFA. This is often easier to use, because the number will match the code it is annotating.
<code>.cfi_remember_state</code>	The <code>.cfi_remember_state</code> directive, saves all the current rules for all the registers. If the following <code>.cfi_*</code> directives is bad, then you can use the <code>.cfi_restore_state</code> directive to restore the previous saved state.
<code>.cfi_restore REGISTER</code>	The <code>.cfi_restore</code> directive, indicates that the rule for register is now the same as it was at the beginning of the function, after all initial instructions added by <code>.cfi_startproc</code> directive are executed.
<code>.cfi_restore_state</code>	The <code>.cfi_restore_state</code> directive, restores the previous saved state of the register.
<code>.cfi_return_column REGISTER</code>	The <code>.cfi_return_column</code> directive, changes return column <code>REGISTER</code> . The return address is either directly in <code>REGISTER</code> or can be accessed by rules for <code>REGISTER</code> .
<code>.cfi_same_value REGISTER</code>	The <code>.cfi_same_value</code> directive, indicates the current value of <code>REGISTER</code> is the same like in the previous frame and does not require restoration.
<code>.cfi_sections section_list</code>	The <code>.cfi_sections section_list</code> directive, specifies if CFI directives should emit <code>.eh_frame</code> section and/or <code>.debug_frame</code> section. You can use <code>.eh_frame</code> as the <code>section_list</code> to emit <code>.eh_frame</code> . You can use the <code>.debug_frame</code> as the <code>section_list</code> to emit <code>.debug_frame</code> . To emit both use <code>.eh_frame</code> and <code>.debug_frame</code> as the <code>section_list</code> . By default, <code>.cfi_sections</code> emits <code>.eh_frame</code> .
<code>.cfi_startproc</code>	The <code>.cfi_startproc</code> directive, is used at the beginning of each function that should have an entry in <code>.eh_frame</code> . It initializes some internal data structures and emits architecture dependent initial CFI instructions. Each <code>.cfi_startproc</code> directive has to be closed by <code>.cfi_endproc</code> .
<code>.cfi_undefined REGISTER</code>	The <code>.cfi_undefined</code> directive, indicates the point from which the previous value of the register cannot be restored.
<code>.comm name, size,alignment</code>	The <code>.comm</code> directive allocates storage in the data section. The storage is referenced by the identifier <code>name</code> . <code>Size</code> is measured in bytes and must

be a positive integer. *Name* cannot be predefined. *Alignment* is optional. If *alignment* is specified, the address of *name* is aligned to a multiple of *alignment*.

<code>.data</code>	The <code>.data</code> directive changes the current section to <code>.data</code> .
<code>.double float</code>	The <code>.double</code> directive generates a double-precision floating-point constant into the current section. The <code>.double</code> directive is not valid for the <code>.bss</code> section.
<code>.even</code>	The <code>.even</code> directive aligns the current program counter (.) to an even boundary.
<code>.ext expression1, expression2, ..., expressionN</code>	The <code>.ext</code> directive generates an 80387 80-bit floating point constant for each <i>expression</i> into the current section. The <code>.ext</code> directive is not valid for the <code>.bss</code> section.
<code>.file "string"</code>	The <code>.file</code> directive creates a symbol table entry where <i>string</i> is the symbol name and <code>STT_FILE</code> is the symbol table type. <i>String</i> specifies the name of the source file associated with the object file.
<code>.float float</code>	The <code>.float</code> directive generates a single-precision floating-point constant into the current section. The <code>.float</code> directive is not valid in the <code>.bss</code> section.
<code>.globl symbol1, symbol2, ..., symbolN</code>	The <code>.globl</code> directive declares each <i>symbol</i> in the list to be <i>global</i> . Each symbol is either defined externally or defined in the input file and accessible in other files. Default bindings for the symbol are overridden. A global symbol definition in one file satisfies an undefined reference to the same global symbol in another file. Multiple definitions of a defined global symbol are not allowed. If a defined global symbol has more than one definition, an error occurs. The <code>.globl</code> directive only declares the symbol to be global in scope, it does not define the symbol.
<code>.group group, section, #comdat</code>	The <code>.group</code> directive adds <i>section</i> to a COMDAT <i>group</i> . Refer to “COMDAT Section” in “Oracle Solaris 11.2 Linkers and Libraries Guide” for additional information about COMDAT.
<code>.hidden symbol1, symbol2, ..., symbolN</code>	The <code>.hidden</code> directive declares each <i>symbol</i> in the list to have <i>hidden</i> linker scoping. All references to <i>symbol</i> within a dynamic module bind to the definition within that module. <i>Symbol</i> is not visible outside of the module.
<code>.ident "string"</code>	The <code>.ident</code> directive creates an entry in the <code>.comment</code> section containing <i>string</i> . <i>String</i> is any sequence of characters, not including the double

	quote ("). To include the double quote character within a string, precede the double quote character with a backslash (\) (ASCII 0x5C).
<code>.lcomm name, size, alignment</code>	The <code>.lcomm</code> directive allocates storage in the <code>.bss</code> section. The storage is referenced by the symbol <i>name</i> , and has a size of <i>size</i> bytes. <i>Name</i> cannot be predefined, and <i>size</i> must be a positive integer. If <i>alignment</i> is specified, the address of <i>name</i> is aligned to a multiple of <i>alignment</i> bytes. If <i>alignment</i> is not specified, the default alignment is 4 bytes.
<code>.local symbol1, symbol2, ..., symbolN</code>	The <code>.local</code> directive declares each <i>symbol</i> in the list to be <i>local</i> . Each symbol is defined in the input file and not accessible to other files. Default bindings for the symbols are overridden. Symbols declared with the <code>.local</code> directive take precedence over <i>weak</i> and <i>global</i> symbols. (See “Symbol Table Section” in “Oracle Solaris 11.2 Linkers and Libraries Guide” for a description of global and weak symbols.) Because local symbols are not accessible to other files, local symbols of the same name may exist in multiple files. The <code>.local</code> directive only declares the symbol to be local in scope, it does not define the symbol.
<code>.long expression1, expression2, ..., expressionN</code>	The <code>.long</code> directive generates a long integer (32-bit, two's complement value) for each <i>expression</i> into the current section. Each <i>expression</i> must be a 32-bit value and must evaluate to an integer value. The <code>.long</code> directive is not valid for the <code>.bss</code> section.
<code>.popsection</code>	The <code>.popsection</code> directive pops the top of the section stack and continues processing of the popped section.
<code>.previous</code>	The <code>.previous</code> directive continues processing of the previous section.
<code>.pushsection section</code>	The <code>.pushsection</code> directive pushes the specified section onto the section stack and switches to another section.
<code>.quad expression1, expression2, ..., expressionN</code>	The <code>.quad</code> directive generates an initialized word (64-bit, two's complement value) for each <i>expression</i> into the current section. Each <i>expression</i> must be a 64-bit value, and must evaluate to an integer value. The <code>.quad</code> directive is not valid for the <code>.bss</code> section.
<code>.rel symbol@ type</code>	The <code>.rel</code> directive generates the specified relocation entry <i>type</i> for the specified <i>symbol</i> . The <code>.lit</code> directive supports TLS (thread-local storage). Refer to Chapter 14, “Thread-Local Storage,” in “Oracle Solaris 11.2 Linkers and Libraries Guide” for additional information about TLS.
<code>.section section, attributes</code>	The <code>.section</code> directive makes <i>section</i> the current section. If <i>section</i> does not exist, a new section with the specified name and attributes is created.

	If <i>section</i> is a non-reserved section, <i>attributes</i> must be included the first time <i>section</i> is specified by the <code>.section</code> directive.
<code>.set symbol, expression</code>	The <code>.set</code> directive assigns the value of <i>expression</i> to <i>symbol</i> . <i>Expression</i> can be any legal expression that evaluates to a numerical value.
<code>.size symbol, expr</code>	Declares the symbol size to be <i>expr</i> . <i>expr</i> must be an absolute expression.
<code>.skip integer, value</code>	While generating values for any data section, the <code>.skip</code> directive causes <i>integer</i> bytes to be skipped over, or, optionally, filled with the specified <i>value</i> .
<code>.sleb128 expression</code>	The <code>.sleb128</code> directive generates a signed, little-endian, base 128 number from <i>expression</i> .
<code>.string "string"</code>	The <code>.string</code> directive places the characters in <i>string</i> into the object module at the current location and terminates the string with a null byte (0). <i>String</i> must be enclosed in double quotes (") (ASCII 0x22). The <code>.string</code> directive is not valid for the <code>.bss</code> section.
<code>.symbolic symbol1, symbol2, ..., symbolN</code>	The <code>.symbolic</code> directive declares each <i>symbol</i> in the list to have <i>symbolic</i> linker scoping. All references to <i>symbol</i> within a dynamic module bind to the definition within that module. Outside of the module, <i>symbol</i> is treated as global.
<code>.tbss</code>	The <code>.tbss</code> directive changes the current section to <code>.tbss</code> . The <code>.tbss</code> section contains uninitialized TLS data objects that will be initialized to zero by the runtime linker.
<code>.tcomm</code>	The <code>.tcomm</code> directive defines a TLS common block.
<code>.tdata</code>	The <code>.tdata</code> directive changes the current section to <code>.tdata</code> . The <code>.tdata</code> section contains the initialization image for initialized TLS data objects.
<code>.text</code>	The <code>.text</code> directive defines the current section as <code>.text</code> .
<code>.type symbol[, symbol, ..., symbol], type[, visibility]</code>	Declares the type of symbol, where <i>type</i> can be: <pre>#object #tls_object #function #no_type</pre> and where <i>visibility</i> can be one of: <pre>#hidden #protected #eliminate #singleton #exported #internal</pre>
<code>.uleb128 expression</code>	The <code>.uleb128</code> directive generates an unsigned, little-endian, base 128 number from <i>expression</i> .

`.value`
expression1,
expression2, ...,
expressionN

The `.value` directive generates an initialized word (16-bit, two's complement value) for each *expression* into the current section. Each *expression* must be a 16-bit integer value. The `.value` directive is not valid for the `.bss` section.

`.weak` *symbol1*,
symbol2, ...,
symbolN

The `.weak` directive declares each *symbol* in the argument list to be defined either externally or in the input file and accessible to other files. Default bindings of the symbol are overridden by the `.weak` directive. A *weak* symbol definition in one file satisfies an undefined reference to a global symbol of the same name in another file. Unresolved *weak* symbols have a default value of zero. The link editor does not resolve these symbols. If a *weak* symbol has the same name as a defined *global* symbol, the weak symbol is ignored and no error results. The `.weak` directive does not define the symbol.

`.zero` *expression*

While filling a data section, the `.zero` directive fills the number of bytes specified by *expression* with zero (0).

Instruction Set Mapping

This chapter provides a general mapping between the Oracle Solaris x86 assembly language mnemonics and the Intel or Advanced Micro Devices (AMD) mnemonics. Refer to [Table 3-1](#) for details on individual processor instructions.

- “3.1 Instruction Overview” on page 28
- “3.2 General-Purpose Instructions” on page 29
- “3.3 Floating-Point Instructions” on page 42
- “3.4 SIMD State Management Instructions” on page 48
- “3.5 AES Instructions” on page 48
- “3.6 AVX Instructions” on page 49
- “3.7 AVX2 Instructions” on page 74
- “3.8 BMI1 Instructions” on page 82
- “3.9 BMI2 Instructions” on page 82
- “3.10 F16C Instructions” on page 83
- “3.11 FMA Instructions” on page 83
- “3.12 FSGSBASE Instructions” on page 90
- “3.13 MMX Instructions” on page 90
- “3.14 MOVBE Instructions” on page 95
- “3.15 PCLMULQDQ Instructions” on page 95
- “3.16 RDRAND Instructions” on page 95
- “3.17 SSE Instructions” on page 95
- “3.18 SSE2 Instructions” on page 103
- “3.19 SSE3 Instructions” on page 111
- “3.20 SSE4a Instructions” on page 112
- “3.21 SSE4.1 Instructions” on page 112
- “3.22 SSE4.2 Instructions” on page 115
- “3.23 SSSE3 Instructions” on page 115
- “3.24 Transactional Synchronization Extensions” on page 116
- “3.25 Operating System Support Instructions” on page 117
- “3.26 VMX Instructions” on page 118
- “3.27 XSAVE Instructions” on page 119

- [“3.28 3DNow Instructions” on page 119](#)
- [“3.29 3DNowx Instructions” on page 121](#)
- [“3.30 64–Bit AMD Opteron Considerations” on page 121](#)

3.1 Instruction Overview

It is beyond the scope of this manual to document the x86 architecture instruction set. This chapter provides a general mapping between the Oracle Solaris x86 assembly language mnemonics and the Intel or AMD mnemonics to enable you to refer to the Intel or AMD documentation for detailed information about a specific instruction. Instructions are listed in tables with the following sections:

- Oracle Solaris mnemonic
- Intel/AMD mnemonic
- Description (short)
- Notes
- Reference

The reference column lists the page number and code for the Intel or AMD manual that documents the instruction. See [Table 3-1](#) for the codes and links to the associated manuals.

For certain Oracle Solaris mnemonics, the allowed data type suffixes for that mnemonic are indicated in braces ({}), following the mnemonic. For example, `bswap{1q}` indicates that the following mnemonics are valid: `bswap`, `bswap1` (which is the default and equivalent to `bswap`), and `bswapq`. See [“2.2.1 Instructions” on page 17](#) for information on data type suffixes.

TABLE 3-1 Instruction References

Manual Code	Name of the Document	Volume	Link
253666-048US/Sep.2013	Intel 64 and IA-32 Architectures Software Developer's Manual	2A	Instruction Set Reference, A-M
253667-048US/Sep.2013	Intel 64 and IA-32 Architectures Software Developer's Manual	2B	Instruction Set Reference, N-Z
326019-048US/Sep.2013	Intel 64 and IA-32 Architectures Software	3C	System Programming Guide, Part 3

Manual Code	Name of the Document	Volume	Link
	Developer's Manual		
319433-016/Oct.2013	Intel Architecture Instruction Set Extensions Programming Reference	-	Intel Architecture Instruction Set Extensions Programming Reference
AMD: 24594-Rev.3.20-May.2013	AMD64 Architecture Programmer's Manual	3	General-Purpose and System Instructions
AMD: 26568-Rev.3.18-Oct.2013	AMD64 Architecture Programmer's Manual	4	128-Bit and 256-Bit Media Instructions
AMD: 26569-Rev.3.13-May.2013	AMD64 Architecture Programmer's Manual	5	64-Bit Media and x87 Floating-Point Instructions

To locate a specific Oracle Solaris x86 mnemonic, look up the mnemonic in the index.

3.2 General-Purpose Instructions

The general-purpose instructions perform basic data movement, memory addressing, arithmetic and logical operations, program flow control, input/output, and string operations on integer, pointer, and BCD data types.

3.2.1 Data Transfer Instructions

The data transfer instructions move data between memory and the general-purpose and segment registers, and perform operations such as conditional moves, stack access, and data conversion.

TABLE 3-2 Data Transfer Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
bswap{lq}	BSWAP	byte swap	bswapq valid only under -m64
cbtw	CBW	convert byte to word	

3.2 General-Purpose Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
<code>cld</code>	CDQ	convert doubleword to quadword	<code>%eax → %edx:%eax</code>
<code>cltq</code>	CDQE	convert doubleword to quadword	<code>%eax → %rax</code> <code>cltq</code> valid only under <code>-m64</code>
<code>cmova{wlq}, cmov{wlq}.a</code>	CMOVA	conditional move if above	<code>cmovaq</code> valid only under <code>-m64</code>
<code>cmovae{wlq}, cmov{wlq}.ae</code>	CMOVAE	conditional move if above or equal	<code>cmovaeq</code> valid only under <code>-m64</code>
<code>cmovb{wlq}, cmov{wlq}.b</code>	CMOVB	conditional move if below	<code>cmovbq</code> valid only under <code>-m64</code>
<code>cmovbe{wlq}, cmov{wlq}.be</code>	CMOVBE	conditional move if below or equal	<code>cmovbeq</code> valid only under <code>-m64</code>
<code>cmovc{wlq}, cmov{wlq}.c</code>	CMOVC	conditional move if carry	<code>cmovcq</code> valid only under <code>-m64</code>
<code>cmove{wlq}, cmov{wlq}.e</code>	CMOVE	conditional move if equal	<code>cmoveq</code> valid only under <code>-m64</code>
<code>cmovg{wlq}, cmov{wlq}.g</code>	CMOVG	conditional move if greater	<code>cmovgq</code> valid only under <code>-m64</code>
<code>cmovge{wlq}, cmov{wlq}.ge</code>	CMOVGE	conditional move if greater or equal	<code>cmovgeq</code> valid only under <code>-m64</code>
<code>cmovl{wlq}, cmov{wlq}.l</code>	CMOVL	conditional move if less	<code>cmovlq</code> valid only under <code>-m64</code>
<code>cmovle{wlq}, cmov{wlq}.le</code>	CMOVLE	conditional move if less or equal	<code>cmovleq</code> valid only under <code>-m64</code>
<code>cmovna{wlq}, cmov{wlq}.na</code>	CMOVNA	conditional move if not above	<code>cmovnaq</code> valid only under <code>-m64</code>
<code>cmovnae{wlq}, cmov{wlq}.nae</code>	CMOVNAE	conditional move if not above or equal	<code>cmovnaeq</code> valid only under <code>-m64</code>
<code>cmovnb{wlq}, cmov{wlq}.nb</code>	CMOVNB	conditional move if not below	<code>cmovnbq</code> valid only under <code>-m64</code>
<code>cmovnbe{wlq}, cmov{wlq}.nbe</code>	CMOVNBE	conditional move if not below or equal	<code>cmovnbeq</code> valid only under <code>-m64</code>
<code>cmovnc{wlq}, cmov{wlq}.nc</code>	CMOVNC	conditional move if not carry	<code>cmovncq</code> valid only under <code>-m64</code>
<code>cmovne{wlq}, cmov{wlq}.ne</code>	CMOVNE	conditional move if not equal	<code>cmovneq</code> valid only under <code>-m64</code>

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
<code>cmovng{wlq}, cmov{wlq}.ng</code>	CMOVNG	conditional move if greater	<code>cmovngq</code> valid only under <code>-m64</code>
<code>cmovnge{wlq}, cmov{wlq}.nge</code>	CMOVNGE	conditional move if not greater or equal	<code>cmovngeq</code> valid only under <code>-m64</code>
<code>cmovnl{wlq}, cmov{wlq}.nl</code>	CMOVNL	conditional move if not less	<code>cmovnlq</code> valid only under <code>-m64</code>
<code>cmovnle{wlq}, cmov{wlq}.nle</code>	CMOVNLE	conditional move if not above or equal	<code>cmovnleq</code> valid only under <code>-m64</code>
<code>cmovno{wlq}, cmov{wlq}.no</code>	CMOVNO	conditional move if not overflow	<code>cmovnoq</code> valid only under <code>-m64</code>
<code>cmovnp{wlq}, cmov{wlq}.np</code>	CMOVNP	conditional move if not parity	<code>cmovnpq</code> valid only under <code>-m64</code>
<code>cmovns{wlq}, cmov{wlq}.ns</code>	CMOVNS	conditional move if not sign (non-negative)	<code>cmovnsq</code> valid only under <code>-m64</code>
<code>cmovnz{wlq}, cmov{wlq}.nz</code>	CMOVNZ	conditional move if not zero	<code>cmovnzq</code> valid only under <code>-m64</code>
<code>cmovo{wlq}, cmov{wlq}. o</code>	CMOVO	conditional move if overflow	<code>cmovoq</code> valid only under <code>-m64</code>
<code>cmovp{wlq}, cmov{wlq}. p</code>	CMOVPP	conditional move if parity	<code>cmovpq</code> valid only under <code>-m64</code>
<code>cmovpe{wlq}, cmov{wlq}. pe</code>	CMOVPE	conditional move if parity even	<code>cmovpeq</code> valid only under <code>-m64</code>
<code>cmovpo{wlq}, cmov{wlq}. po</code>	CMOVPO	conditional move if parity odd	<code>cmovpoq</code> valid only under <code>-m64</code>
<code>cmovs{wlq}, cmov{wlq}.s</code>	CMOVSS	conditional move if sign (negative)	<code>cmovsq</code> valid only under <code>-m64</code>
<code>cmovz{wlq}, cmov{wlq}.z</code>	CMOVZ	conditional move if zero	<code>cmovzq</code> valid only under <code>-m64</code>
<code>cmpxchg{bw}lq</code>	CMPXCHG	compare and exchange	<code>cmpxchgq</code> valid only under <code>-m64</code>
<code>cmpxchg8b</code>	CMPXCHG8B	compare and exchange 8 bytes	
<code>cqtd</code>	CQO	convert quadword to octword	<code>%rax → %rdx:%rax</code> <code>cqtd</code> valid only under <code>-m64</code>
<code>cqto</code>	CQO	convert quadword to octword	<code>%rax → %rdx:%rax</code>

3.2 General-Purpose Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
			cqto valid only under -m64
cwtd	CWD	convert word to doubleword	%ax → %dx:%ax
cwtl	CWDE	convert word to doubleword in %eax register	%ax → %eax
invpcid	INVPCID	Invalidate Process-Context Identifier	page 3-416 (253666-048US/Sep.2013)
mov{bwlq}	MOV	move data between immediate values, general purpose registers, segment registers, and memory	movq valid only under -m64
movabs{bwlq}	MOVABS	move immediate value to register	movabs valid only under -m64
movabs{bwlq}A	MOVABS	move immediate value to register {AL, AX, GAX, RAX}	movabs valid only under -m64
movsb{wlq}, movsw{lq}	MOVSX	move and sign extend	movsbq and movswq valid only under -m64
movzb{wlq}, movzw{lq}	MOVZX	move and zero extend	movzbq and movzwq valid only under -m64
pop{wlq}	POP	pop stack	popq valid only under -m64
popaw	POPA	pop general-purpose registers from stack	popaw invalid under -m64
popal, popa	POPAD	pop general-purpose registers from stack	invalid under -m64
push{wlq}	PUSH	push onto stack	pushq valid only under -m64
pushaw	PUSHA	push general-purpose registers onto stack	pushaw invalid under -m64
pushal, pusha	PUSHAD	push general-purpose registers onto stack	invalid under -m64
xadd{bwlq}	XADD	exchange and add	xaddq valid only under -m64
xchg{bwlq}	XCHG	exchange	xchqq valid only under -m64
xchg{bwlq}A	XCHG	exchange	xchqgA valid only under -m64

3.2.2 Binary Arithmetic Instructions

The binary arithmetic instructions perform basic integer computations on operands in memory or the general-purpose registers.

TABLE 3-3 Binary Arithmetic Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
adc{bwlq}	ADC	add with carry	adcq valid only under -m64
add{bwlq}	ADD	integer add	addq valid only under -m64
cmp{bwlq}	CMP	compare	cmpq valid only under -m64
dec{bwlq}	DEC	decrement	decq valid only under -m64
div{bwlq}	DIV	divide (unsigned)	divq valid only under -m64
idiv{bwlq}	IDIV	divide (signed)	idivq valid only under -m64
imul{bwlq}	IMUL	multiply (signed)	imulq valid only under -m64
inc{bwlq}	INC	increment	incq valid only under -m64
mul{bwlq}	MUL	multiply (unsigned)	mulq valid only under -m64
neg{bwlq}	NEG	negate	negq valid only under -m64
sbb{bwlq}	SBB	subtract with borrow	sbbq valid only under -m64
sub{bwlq}	SUB	subtract	subq valid only under -m64

3.2.3 Decimal Arithmetic Instructions

The decimal arithmetic instructions perform decimal arithmetic on binary coded decimal (BCD) data.

TABLE 3-4 Decimal Arithmetic Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
aaa	AAA	ASCII adjust after addition	invalid under -m64
aad	AAD	ASCII adjust before division	invalid under -m64
aam	AAM	ASCII adjust after multiplication	invalid under -m64

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
aas	AAS	ASCII adjust after subtraction	invalid under -m64
daa	DAA	decimal adjust after addition	invalid under -m64
das	DAS	decimal adjust after subtraction	invalid under -m64

3.2.4 Logical Instructions

The logical instructions perform basic logical operations on their operands.

TABLE 3-5 Logical Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
and{bwlq}	AND	bitwise logical AND	andq valid only under -m64
not{bwlq}	NOT	bitwise logical NOT	notq valid only under -m64
or{bwlq}	OR	bitwise logical OR	orq valid only under -m64
xor{bwlq}	XOR	bitwise logical exclusive OR	xorq valid only under -m64

3.2.5 Shift and Rotate Instructions

The shift and rotate instructions shift and rotate the bits in their operands.

TABLE 3-6 Shift and Rotate Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
rcl{bwlq}	RCL	rotate through carry left	rclq valid only under -m64
rcr{bwlq}	RCR	rotate through carry right	rcrq valid only under -m64
rol{bwlq}	ROL	rotate left	rolq valid only under -m64
ror{bwlq}	ROR	rotate right	rorq valid only under -m64
sal{bwlq}	SAL	shift arithmetic left	salq valid only under -m64
sar{bwlq}	SAR	shift arithmetic right	sarq valid only under -m64
shl{bwlq}	SHL	shift logical left	shlq valid only under -m64

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
shld{bwlq}	SHLD	shift left double	shldq valid only under -m64
shr{bwlq}	SHR	shift logical right	shrq valid only under -m64
shrd{bwlq}	SHRD	shift right double	shrdq valid only under -m64

3.2.6 Bit and Byte Instructions

The bit instructions test and modify individual bits in operands. The byte instructions set the value of a byte operand to indicate the status of flags in the `%eflags` register.

TABLE 3-7 Bit and Byte Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
bsf{wlq}	BSF	bit scan forward	bsfq valid only under -m64
bsr{wlq}	BSR	bit scan reverse	bsrq valid only under -m64
bt{wlq}	BT	bit test	btq valid only under -m64
btc{wlq}	BTC	bit test and complement	btcq valid only under -m64
btr{wlq}	BTR	bit test and reset	btrq valid only under -m64
bts{wlq}	BTS	bit test and set	btsq valid only under -m64
seta	SETA	set byte if above	
setae	SETAE	set byte if above or equal	
setb	SETB	set byte if below	
setbe	SETBE	set byte if below or equal	
setc	SETC	set byte if carry	
sete	SETE	set byte if equal	
setg	SETG	set byte if greater	
setge	SETGE	set byte if greater or equal	
setl	SETL	set byte if less	
setle	SETLE	set byte if less or equal	
setna	SETNA	set byte if not above	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
setnae	SETNAE	set byte if not above or equal	
setnb	SETNB	set byte if not below	
setnbe	SETNBE	set byte if not below or equal	
setnc	SETNC	set byte if not carry	
setne	SETNE	set byte if not equal	
setng	SETNG	set byte if not greater	
setnge	SETNGE	set byte if not greater or equal	
setnl	SETNL	set byte if not less	
setnle	SETNLE	set byte if not less or equal	
setno	SETNO	set byte if not overflow	
setnp	SETNP	set byte if not parity	
setns	SETNS	set byte if not sign (non-negative)	
setnz	SETNZ	set byte if not zero	
seto	SETO	set byte if overflow	
setp	SETP	set byte if parity	
setpe	SETPE	set byte if parity even	
setpo	SETPO	set byte if parity odd	
sets	SETS	set byte if sign (negative)	
setz	SETZ	set byte if zero	
test{bwlq}	TEST	logical compare	testq valid only under -m64

3.2.7 Control Transfer Instructions

The control transfer instructions control the flow of program execution.

TABLE 3-8 Control Transfer Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
bound{wl}	BOUND	detect value out of range	boundw invalid under -m64
call	CALL	call procedure	
enter	ENTER	high-level procedure entry	
int	INT	software interrupt	
into	INTO	interrupt on overflow	invalid under -m64
iret	IRET	return from interrupt	
ja	JA	jump if above	
jae	JAE	jump if above or equal	
jb	JB	jump if below	
jbe	JBE	jump if below or equal	
jc	JC	jump if carry	
jcxz	JCXZ	jump register %cx zero	
je	JE	jump if equal	
jecxz	JECXZ	jump register %ecx zero	invalid under -m64
jg	JG	jump if greater	
jge	JGE	jump if greater or equal	
jl	JL	jump if less	
jle	JLE	jump if less or equal	
jmp	JMP	jump	
jnae	JNAE	jump if not above or equal	
jnb	JNB	jump if not below	
jnbe	JNBE	jump if not below or equal	
jnc	JNC	jump if not carry	
jne	JNE	jump if not equal	
jng	JNG	jump if not greater	
jnge	JNGE	jump if not greater or equal	
jnl	JNL	jump if not less	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
<code>jnl</code>	JNLE	jump if not less or equal	
<code>jno</code>	JNO	jump if not overflow	
<code>jnp</code>	JNP	jump if not parity	
<code>jns</code>	JNS	jump if not sign (non-negative)	
<code>jnz</code>	JNZ	jump if not zero	
<code>jo</code>	JO	jump if overflow	
<code>jp</code>	JP	jump if parity	
<code>jpe</code>	JPE	jump if parity even	
<code>jpo</code>	JPO	jump if parity odd	
<code>js</code>	JS	jump if sign (negative)	
<code>jz</code>	JZ	jump if zero	
<code>lcall</code>	CALL	call far procedure	valid as indirect only for -m64
<code>leave</code>	LEAVE	high-level procedure exit	
<code>loop</code>	LOOP	loop with %ecx counter	
<code>loope</code>	LOOPE	loop with %ecx and equal	
<code>loopne</code>	LOOPNE	loop with %ecx and not equal	
<code>loopnz</code>	LOOPNZ	loop with %ecx and not zero	
<code>loopz</code>	LOOPZ	loop with %ecx and zero	
<code>lret</code>	RET	return from far procedure	valid as indirect only for m64
<code>ret</code>	RET	return	

3.2.8 String Instructions

The string instructions operate on strings of bytes. Operations include storing strings in memory, loading strings from memory, comparing strings, and scanning strings for substrings.

Note - The Oracle Solaris mnemonics for certain instructions differ slightly from the Intel/AMD mnemonics. Alphabetization of the table below is by the Oracle Solaris mnemonic. All string operations default to long (doubleword).

TABLE 3-9 String Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
cmps{q}	CMPS	compare string	cmpsq valid only under -m64
cmpsb	CMPSB	compare byte string	
cmpsl	CMPSD	compare doubleword string	
cmpsw	CMPSW	compare word string	
lods{q}	LODS	load string	lodsq valid only under -m64
lodsb	LODSB	load byte string	
lodsl	LODSD	load doubleword string	
lodsw	LODSW	load word string	
movs{q}	MOVS	move string	movsq valid only under -m64
movsb	MOVSB	move byte string	movsb is not movsb{wlq}. See Table 3-2
movsl, smovl	MOVSD	move doubleword string	
movsw, smovw	MOVSW	move word string	movsw is not movsw{lq}. See Table 3-2
rep	REP	repeat while %ecx not zero	
repnz	REPNE	repeat while not equal	
repnz	REPZ	repeat while not zero	
repz	REPE	repeat while equal	
repz	REPZ	repeat while zero	
scas{q}	SCAS	scan string	scasq valid only under -m64
scasb	SCASB	scan byte string	
scasl	SCASD	scan doubleword string	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
scasw	SCASW	scan word string	
stos{q}	STOS	store string	stosq valid only under -m64
stosb	STOSB	store byte string	
stosl	STOSD	store doubleword string	
stosw	STOSW	store word string	

3.2.9 I/O Instructions

The input/output instructions transfer data between the processor's I/O ports, registers, and memory.

TABLE 3-10 I/O Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
in	IN	read from a port	
ins	INS	input string from a port	
insb	INSB	input byte string from port	
insl	INSD	input doubleword string from port	
insw	INSW	input word string from port	
out	OUT	write to a port	
outs	OUTS	output string to port	
outsb	OUTSB	output byte string to port	
outsl	OUTSD	output doubleword string to port	
outsw	OUTSW	output word string to port	

3.2.10 Flag Control (EFLAG) Instructions

The status flag control instructions operate on the bits in the `%eflags` register.

TABLE 3-11 Flag Control Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
clc	CLC	clear carry flag	
cld	CLD	clear direction flag	
cli	CLI	clear interrupt flag	
cmc	CMC	complement carry flag	
lahf	LAHF	load flags into %ah register	
popfw	POPF	pop %eflags from stack	
popf{lq}	POPFL	pop %eflags from stack	popfq valid only under -m64
pushfw	PUSHF	push %eflags onto stack	
pushf{lq}	PUSHFL	push %eflags onto stack	pushfq valid only under -m64
sahf	SAHF	store %ah register into flags	
stc	STC	set carry flag	
std	STD	set direction flag	
sti	STI	set interrupt flag	

3.2.11 Segment Register Instructions

The segment register instructions load far pointers (segment addresses) into the segment registers.

TABLE 3-12 Segment Register Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
lds{wl}	LDS	load far pointer using %ds	ldsL and ldsw invalid under -m64
les{wl}	LES	load far pointer using %es	lesL and lesw invalid under -m64
lfs{wl}	LFS	load far pointer using %fs	
lgs{wl}	LGS	load far pointer using %gs	
lss{wl}	LSS	load far pointer using %ss	

3.2.12 Miscellaneous Instructions

The instructions documented in this section provide a number of useful functions.

TABLE 3-13 Miscellaneous Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
<code>cputd</code>	CPUID	processor identification	
<code>lea{wlq}</code>	LEA	load effective address	<code>leaq</code> valid only under <code>-m64</code>
<code>nop</code>	NOP	no operation	
<code>ud2</code>	UD2	undefined instruction	
<code>xlat</code>	XLAT	table lookup translation	
<code>xlatb</code>	XLATB	table lookup translation	

3.3 Floating-Point Instructions

The floating point instructions operate on floating-point, integer, and binary coded decimal (BCD) operands.

3.3.1 Data Transfer Instructions (Floating Point)

The data transfer instructions move floating-point, integer, and BCD values between memory and the floating point registers.

TABLE 3-14 Data Transfer Instructions (Floating-Point)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
<code>fbld</code>	FBLD	load BCD	
<code>fbstp</code>	FBSTP	store BCD and pop	
<code>fcmovb</code>	FCMOVB	floating-point conditional move if below	
<code>fcmovbe</code>	FCMOVBE	floating-point conditional move if below or equal	
<code>fcmove</code>	FCMOVE	floating-point conditional move if equal	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
fcmovnb	FCMOVNB	floating-point conditional move if not below	
fcmovnbe	FCMOVNBE	floating-point conditional move if not below or equal	
fcmovne	FCMOVNE	floating-point conditional move if not equal	
fcmovnu	FCMOVNU	floating-point conditional move if unordered	
fcmovu	FCMOVU	floating-point conditional move if unordered	
fild	FILD	load integer	
fist	FIST	store integer	
fistp	FISTP	store integer and pop	
fld	FLD	load floating-point value	
fst	FST	store floating-point value	
fstp	FSTP	store floating-point value and pop	
fxch	FXCH	exchange registers	

3.3.2 Basic Arithmetic Instructions (Floating-Point)

The basic arithmetic instructions perform basic arithmetic operations on floating-point and integer operands.

TABLE 3-15 Basic Arithmetic Instructions (Floating-Point)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
fabs	FABS	absolute value	
fadd	FADD	add floating-point	
faddp	FADDP	add floating-point and pop	
fchs	FCHS	change sign	
fdiv	FDIV	divide floating-point	
fdivp	FDIVP	divide floating-point and pop	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
<code>fdivr</code>	<code>FDIVR</code>	divide floating-point reverse	
<code>fdivrp</code>	<code>FDIVRP</code>	divide floating-point reverse and pop	
<code>fiadd</code>	<code>FIADD</code>	add integer	
<code>fidiv</code>	<code>FIDIV</code>	divide integer	
<code>fidivr</code>	<code>FIDIVR</code>	divide integer reverse	
<code>fimul</code>	<code>FIMUL</code>	multiply integer	
<code>fisub</code>	<code>FISUB</code>	subtract integer	
<code>fisubr</code>	<code>FISUBR</code>	subtract integer reverse	
<code>fmul</code>	<code>FMUL</code>	multiply floating-point	
<code>fmulp</code>	<code>FMULP</code>	multiply floating-point and pop	
<code>fprem</code>	<code>FPREM</code>	partial remainder	
<code>fprem1</code>	<code>FPREM1</code>	IEEE partial remainder	
<code>frndint</code>	<code>FRNDINT</code>	round to integer	
<code>fscale</code>	<code>FSCALE</code>	scale by power of two	
<code>fsqrt</code>	<code>FSQRT</code>	square root	
<code>fsub</code>	<code>FSUB</code>	subtract floating-point	
<code>fsubp</code>	<code>FSUBP</code>	subtract floating-point and pop	
<code>fsubr</code>	<code>FSUBR</code>	subtract floating-point reverse	
<code>fsubrp</code>	<code>FSUBRP</code>	subtract floating-point reverse and pop	
<code>fxtract</code>	<code>FXTRACT</code>	extract exponent and significand	

3.3.3 Comparison Instructions (Floating-Point)

The floating-point comparison instructions operate on floating-point or integer operands.

TABLE 3-16 Comparison Instructions (Floating-Point)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
fcom	FCOM	compare floating-point	
fcomi	FCOMI	compare floating-point and set %eflags	
fcomip	FCOMIP	compare floating-point, set %eflags, and pop	
fcomp	FCOMP	compare floating-point and pop	
fcompp	FCOMPP	compare floating-point and pop twice	
ficom	FICOM	compare integer	
ficomp	FICOMP	compare integer and pop	
ftst	FTST	test floating-point (compare with 0.0)	
fucom	FUCOM	unordered compare floating-point	
fucomi	FUCOMI	unordered compare floating-point and set %eflags	
fucomip	FUCOMIP	unordered compare floating-point, set %eflags, and pop	
fucomp	FUCOMP	unordered compare floating-point and pop	
fucompp	FUCOMPP	compare floating-point and pop twice	
fxam	FXAM	examine floating-point	

3.3.4 Transcendental Instructions (Floating-Point)

The transcendental instructions perform trigonometric and logarithmic operations on floating-point operands.

TABLE 3-17 Transcendental Instructions (Floating-Point)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
f2xm1	F2XM1	computes $2^x - 1$	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
fcos	FCOS	cosine	
fpatan	FPATAN	partial arctangent	
fptan	FPTAN	partial tangent	
fsin	FSIN	sine	
fsincos	FSINCOS	sine and cosine	
fyl2x	FYL2X	computes $y * \log_2 x$	
fyl2xp1	FYL2XP1	computes $y * \log_2(x+1)$	

3.3.5 Load Constants (Floating-Point) Instructions

The load constants instructions load common constants, such as π , into the floating-point registers.

TABLE 3-18 Load Constants Instructions (Floating-Point)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
fld1	FLD1	load +1.0	
fldl2e	FLDL2E	load $\log_2 e$	
fldl2t	FLDL2T	load $\log_2 10$	
fldlg2	FLDLG2	load $\log_{10} 2$	
fldln2	FLDLN2	load $\log_e 2$	
fldpi	FLDPI	load π	
fldz	FLDZ	load +0.0	

3.3.6 Control Instructions (Floating-Point)

The floating-point control instructions operate on the floating-point register stack and save and restore the floating-point state.

TABLE 3-19 Control Instructions (Floating-Point)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
fclex	FCLEX	clear floating-point exception flags after	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
		checking for error conditions	
fdecstp	FDECSTP	decrement floating-point register stack pointer	
ffree	FFREE	free floating-point register	
fincstp	FINCSTP	increment floating-point register stack pointer	
finit	FINIT	initialize floating-point unit after checking error conditions	
fldcw	FLDCW	load floating-point unit control word	
fldenv	FLDENV	load floating-point unit environment	
fnclex	FNCLEX	clear floating-point exception flags without checking for error conditions	
fninit	FNINIT	initialize floating-point unit without checking error conditions	
fnop	FNOP	floating-point no operation	
fnsave	FNSAVE	save floating-point unit state without checking error conditions	
fnstcw	FNSTCW	store floating-point unit control word without checking error conditions	
fnstenv	FNSTENV	store floating-point unit environment without checking error conditions	
fnstsw	FNSTSW	store floating-point unit status word without checking error conditions	
frstor	FRSTOR	restore floating-point unit state	
fsave	FSAVE	save floating-point unit state after checking error conditions	

3.4 SIMD State Management Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
fstcw	FSTCW	store floating-point unit control word after checking error conditions	
fstenv	FSTENV	store floating-point unit environment after checking error conditions	
fstsw	FSTSW	store floating-point unit status word after checking error conditions	
fwait	FWAIT	wait for floating-point unit	
wait	WAIT	wait for floating-point unit	

3.4 SIMD State Management Instructions

The `fxsave` and `fxrstor` instructions save and restore the state of the floating-point unit and the MMX, XMM, and MXCSR registers.

TABLE 3-20 SIMD State Management Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
fxrstor	FXRSTOR	restore floating-point unit and SIMD state	
fxsave	FXSAVE	save floating-point unit and SIMD state	

3.5 AES Instructions

TABLE 3-21 AES Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
aesdec	AESDEC	Perform One Round of an AES Decryption Flow	page 3-40 (253666-048US/Sep.2013)
aesdeclast	AESDECLAST	Perform Last Round of an AES Decryption Flow	page 3-42 (253666-048US/Sep.2013)
aesenc	AESENC	Perform One Round of an AES Encryption Flow	page 3-44 (253666-048US/Sep.2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
aesenclast	AESENCLAST	Perform Last Round of an AES Encryption Flow	page 3-46 (253666-048US/Sep.2013)
aesimc	AESIMC	Perform the AES InvMix Column Transformation	page 3-48 (253666-048US/Sep.2013)
aeskeygenassist	AESKEYGENASSIST	AES Round Key Generation Assist	page 3-49 (253666-048US/Sep.2013)

3.5.1 Advanced Vector Extensions of AES Instructions

TABLE 3-22 Advanced Vector Extensions of AES Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vaesdec	AESDEC	Perform One Round of an AES Decryption Flow	page 3-40 (253666-048US/Sep.2013)
vaesdeclast	AESDECLAST	Perform Last Round of an AES Decryption Flow	page 3-42 (253666-048US/Sep.2013)
vaesenc	AESENC	Perform One Round of an AES Encryption Flow	page 3-44 (253666-048US/Sep.2013)
vaesenclast	AESENCLAST	Perform Last Round of an AES Encryption Flow	page 3-46 (253666-048US/Sep.2013)
vaesimc	AESIMC	Perform the AES InvMix Column Transformation	page 3-48 (253666-048US/Sep.2013)
vaeskeygenassist	AESKEYGENASSIST	AES Round Key Generation Assist	page 3-49 (253666-048US/Sep.2013)

3.6 AVX Instructions

TABLE 3-23 AVX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vaddpd	ADDPD	Add Packed Double-Precision Floating-Point Values	page 5-7 (319433-016/Oct.2013)
vaddps	ADDPS	Add Packed Single-Precision Floating-Point Values	page 5-10 (319433-016/Oct.2013)

3.6 AVX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vaddsd	ADDSD	Add Scalar Double-Precision Floating-Point Values	page 5-13 (319433-016/Oct. 2013)
vaddss	ADDSS	Add Scalar Single-Precision Floating-Point Values	page 5-15 (319433-016/Oct. 2013)
vaddsubpd	ADDSUBPD	Packed Double-FP Add/Subtract	page 3-35 (253666-048US/Sep.2013)
vaddsubps	ADDSUBPS	Packed Single-FP Add/Subtract	page 3-37 (253666-048US/Sep.2013)
vandnpd	ANDNPD	Bitwise Logical AND NOT of Packed Double-Precision Floating-Point Values	page 3-58 (253666-048US/Sep.2013)
vandnps	ANDNPS	Bitwise Logical AND NOT of Packed Single-Precision Floating-Point Values	page 3-60 (253666-048US/Sep.2013)
vandpd	ANDPD	Bitwise Logical AND of Packed Double-Precision Floating-Point Values	page 3-54 (253666-048US/Sep.2013)
vandps	ANDPS	Bitwise Logical AND of Packed Single-Precision Floating-Point Values	page 3-56 (253666-048US/Sep.2013)
vblendpd	BLENDPD	Blend Packed Double Precision Floating-Point Values	page 3-64 (253666-048US/Sep.2013)
vblendps	BLENDPS	Blend Packed Single Precision Floating-Point Values	page 3-68 (253666-048US/Sep.2013)
vblendvpd	BLENDVPD	Variable Blend Packed Double Precision Floating-Point Values	page 3-70 (253666-048US/Sep.2013)
vblendvps	BLENDVPS	Variable Blend Packed Single Precision Floating-Point Values	page 3-72 (253666-048US/Sep.2013)
vcmpeq_ospd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpeq_uqpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vcmpcq_ospd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpcpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpfalse_ospd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpfalsepd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpge_oqpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpgepd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpgt_oqpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpgtpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmple_oqpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmplepd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmplt_oqpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpltpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpneq_oqpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpneq_ospd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)

3.6 AVX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vcmpneq_uspd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpneqpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpnge_uqpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpngepd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpngt_uqpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpngtpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpnl_e_uqpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpnl_e_qpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpnl_t_uqpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpnl_t_qpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpord_spd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpordpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpdpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmptrue_uspd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vcmptruepd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpunord_spd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpunordpd	CMPPD	Compare Packed Double-Precision Floating-Point Values	page 5-40 (319433-016/Oct. 2013)
vcmpseq_osps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpseq_uqps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpseq_usps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpseqps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpfalse_osps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpfalseps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpge_oqps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpgeps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpgt_oqps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpgtps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmple_oqps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)

3.6 AVX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vcmpleps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmplt_oqps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpltps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpneq_oqps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpneq_osps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpneq_usps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpneqps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpnge_uqps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpngeps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpngt_uqps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpngtps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpnl_e_uqps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpnl_eps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpnlt_uqps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vcmpnltps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpord_sps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpordps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmppps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmptrue_usps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmptrueps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpunord_sps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpunordps	CMPPS	Compare Packed Single-Precision Floating-Point Values	page 5-46 (319433-016/Oct. 2013)
vcmpeq_ossd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpeq_uqsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpeq_ussd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpeqsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpfalse_ossd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpfalse_ssd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)

3.6 AVX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vcmpge_qlsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpgesd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpgt_qlsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpgtsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmple_qlsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpleqd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmplt_qlsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpltsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpneq_qlsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpneq_qlssd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpneq_qlssd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpneqsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpnge_qlsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpngesd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vcmpngt_uqsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpngtsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpnle_uqsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpnlesd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpnlt_uqsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpnltsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpord_ssd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpordsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmptrue_ussd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmptruesd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpunord_ssd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpunordsd	CMPSD	Compare Scalar Double-Precision Floating-Point Value	page 5-52 (319433-016/Oct. 2013)
vcmpeq_oss	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)

3.6 AVX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vcmpeq_uqss	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpeq_uss	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpeqss	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpfalse_oss	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpfalse	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpge_oqss	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpge	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpgt_oqss	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpgt	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmple_oqss	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmple	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpplt_oqss	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpplt	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpneq_oqss	CMPSQ	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vcmpneq_oss	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpneq_uss	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpneqss	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpnge_uqss	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpngess	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpngt_uqss	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpngtss	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpnle_uqss	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpnless	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpnlt_uqss	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpnltss	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpord_oss	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpordss	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
vcmpss	CMPS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)

3.6 AVX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
<code>vcmptrue_usss</code>	CMPSS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
<code>vcmptrue_ss</code>	CMPSS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
<code>vcmpunord_sss</code>	CMPSS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
<code>vcmpunord_ss</code>	CMPSS	Compare Scalar Single-Precision Floating-Point Value	page 5-57 (319433-016/Oct. 2013)
<code>vcomisd</code>	COMISD	Compare Scalar Ordered Double-Precision Floating-Point Values and Set EFLAGS	page 5-62 (319433-016/Oct. 2013)
<code>vcomiss</code>	COMISS	Compare Scalar Ordered Single-Precision Floating-Point Values and Set EFLAGS	page 5-64 (319433-016/Oct. 2013)
<code>vcvtdq2pd</code>	CVTDQ2PD	Convert Packed Doubleword Integers to Packed Double-Precision Floating-Point Values	page 5-79 (319433-016/Oct. 2013)
<code>vcvtdq2ps</code>	CVTDQ2PS	Convert Packed Doubleword Integers to Packed Single-Precision Floating-Point Values	page 5-82 (319433-016/Oct. 2013)
<code>vcvtpd2dq(x y)</code>	CVTPD2DQ	Convert Packed Double-Precision Floating-Point Values to Packed Doubleword Integers	page 5-85 (319433-016/Oct. 2013)
<code>vcvtpd2ps(x y)</code>	CVTPD2PS	Convert Packed Double-Precision Floating-Point Values to Packed Single-Precision Floating-Point Values	page 5-88 (319433-016/Oct. 2013)
<code>vcvtps2dq</code>	CVTPS2DQ	Convert Packed Single-Precision Floating-Point Values to Packed Signed Doubleword Integer Values	page 5-100 (319433-016/Oct. 2013)
<code>vcvtps2pd</code>	CVTPS2PD	Convert Packed Single-Precision Floating-Point	page (319433-016/Oct.2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
		Values to Packed Double-Precision Floating-Point	
<code>vcvtsd2si(q l)</code>	CVTSD2SI	Convert Scalar Double-Precision Floating-Point Value to Doubleword Integer	page 5-108 (319433-016/Oct. 2013)
<code>vcvtsd2ss</code>	CVTSD2SS	Convert Scalar Double-Precision Floating-Point Value to Scalar Single-Precision Floating-Point Value	page 5-112 (319433-016/Oct. 2013)
<code>vcvtss2sd(q l)</code>	CVTSS2SD	Convert Doubleword Integer to Scalar Double-Precision Floating-Point Value	page 5-114 (319433-016/Oct. 2013)
<code>vcvtss2ss(q l)</code>	CVTSS2SS	Convert Doubleword Integer to Scalar Single-Precision Floating-Point Value	page 5-116 (319433-016/Oct. 2013)
<code>vcvtss2sd</code>	CVTSS2SD	Convert Scalar Single-Precision Floating-Point Value to Scalar Double-Precision Floating-Point Value	page 5-118 (319433-016/Oct. 2013)
<code>vcvtss2si(q l)</code>	CVTSS2SI	Convert Scalar Single-Precision Floating-Point Value to Doubleword Integer	page 5-120 (319433-016/Oct. 2013)
<code>vcvttpd2dq(x y)</code>	CVTTPD2DQ	Convert with Truncation Packed Double-Precision Floating-Point Values to Packed Doubleword	page (319433-016/Oct.2013)
<code>vcvttps2dq</code>	CVTTPS2DQ	Convert with Truncation Packed Single-Precision Floating-Point Values to Packed Signed Doubleword	page (319433-016/Oct.2013)
<code>vcvttsd2si(q l)</code>	CVTTS2SI	Convert with Truncation Scalar Double-Precision Floating-Point Value to Signed Integer	page 5-134 (319433-016/Oct. 2013)
<code>vcvtts2si(q l)</code>	CVTTS2SI	Convert with Truncation Scalar Single-Precision Floating-Point Value to Integer	page 5-137 (319433-016/Oct. 2013)

3.6 AVX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vdivpd	DIVPD	Divide Packed Double-Precision Floating-Point Values	page 5-66 (319433-016/Oct. 2013)
vdivps	DIVPS	Divide Packed Single-Precision Floating-Point Values	page 5-68 (319433-016/Oct. 2013)
vdivsd	DIVSD	Divide Scalar Double-Precision Floating-Point Value	page 5-71 (319433-016/Oct. 2013)
vdivss	DIVSS	Divide Scalar Single-Precision Floating-Point Values	page 5-73 (319433-016/Oct. 2013)
vdppd	DPPD	Dot Product of Packed Double Precision Floating-Point Values	page 3-240 (253666-048US/Sep.2013)
vdpps	DPPS	Dot Product of Packed Single Precision Floating-Point Values	page 3-242 (253666-048US/Sep.2013)
vextractps	EXTRACTPS	Extract Packed Floating-Point Values	page 5-158 (319433-016/Oct. 2013)
vhaddpd	HADDPD	Packed Double-FP Horizontal Add	page 3-370 (253666-048US/Sep.2013)
vhaddps	HADDPS	Packed Single-FP Horizontal Add	page 3-373 (253666-048US/Sep.2013)
vhsubpd	HSUBPD	Packed Double-FP Horizontal Subtract	page 3-377 (253666-048US/Sep.2013)
vhsubps	HSUBPS	Packed Single-FP Horizontal Subtract	page 3-380 (253666-048US/Sep.2013)
vinsertps	INSERTPS	Insert Scalar Single-Precision Floating-Point Value	page 5-311 (319433-016/Oct. 2013)
vlddqu	LDDQU	Load Unaligned Integer 128 Bits	page 3-444 (253666-048US/Sep.2013)
vldmxcsr	LDMXCSR	Load MXCSR Register	page 3-446 (253666-048US/Sep.2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vmaskovdqu	MASKMOVDQU	Store Selected Bytes of Double Quadword	page 3-478 (253666-048US/ Sep.2013)
vmaxpd	MAXPD	Maximum of Packed Double-Precision Floating-Point Values	page 5-314 (319433-016/Oct. 2013)
vmaxps	MAXPS	Maximum of Packed Single-Precision Floating-Point Values	page 5-317 (319433-016/Oct. 2013)
vmaxsd	MAXSD	Return Maximum Scalar Double-Precision Floating-Point Value	page 5-320 (319433-016/Oct. 2013)
vmaxss	MAXSS	Return Maximum Scalar Single-Precision Floating-Point Value	page 5-322 (319433-016/Oct. 2013)
vminpd	MINPD	Minimum of Packed Double-Precision Floating-Point Values	page 5-324 (319433-016/Oct. 2013)
vminps	MINPS	Minimum of Packed Single-Precision Floating-Point Values	page 5-327 (319433-016/Oct. 2013)
vminsd	MINSO	Return Minimum Scalar Double-Precision Floating-Point Value	page 5-330 (319433-016/Oct. 2013)
vminss	MINSS	Return Minimum Scalar Single-Precision Floating-Point Value	page 5-332 (319433-016/Oct. 2013)
vmovapd	MOVAPD	Move Aligned Packed Double-Precision Floating-Point Values	page 5-334 (319433-016/Oct. 2013)
vmovaps	MOVAPS	Move Aligned Packed Single-Precision Floating-Point Values	page 5-337 (319433-016/Oct. 2013)
vmov(q d)	MOVDMOVQ	Move Doubleword and Quadword	page 5-340 (319433-016/Oct. 2013)
vmovddup	MOVDDUP	Replicate Double FP Values	page 5-346 (319433-016/Oct. 2013)
vmovdqa	MOVQQA	Move Aligned Packed Integer Values	page 5-349 (319433-016/Oct. 2013)

3.6 AVX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vmovdqu	MOVDQU VMOVDQU32 VMOVDQU64	Move Unaligned Packed Integer Values	page 5-353 (319433-016/Oct. 2013)
vmovhlps	MOVHLP	Move Packed Single-Precision Floating-Point Values High to Low	page 5-357 (319433-016/Oct. 2013)
vmovhpd	MOVHPD	Move High Packed Double-Precision Floating-Point Values	page 5-359 (319433-016/Oct. 2013)
vmovhps	MOVHPS	Move High Packed Single-Precision Floating-Point Values	page 5-361 (319433-016/Oct. 2013)
vmovlhps	MOVLHPS	Move Packed Single-Precision Floating-Point Values Low to High	page 5-363 (319433-016/Oct. 2013)
vmovlpd	MOVLPD	Move Low Packed Double-Precision Floating-Point Values	page 5-365 (319433-016/Oct. 2013)
vmovlps	MOVLPS	Move Low Packed Single-Precision Floating-Point Values	page 5-367 (319433-016/Oct. 2013)
vmovmskpd	MOVMSKPD	Extract Packed Double-Precision Floating-Point Sign Mask	page 3-539 (253666-048US/Sep.2013)
vmovmskps	MOVMSKPS	Extract Packed Single-Precision Floating-Point Sign Mask	page 3-541 (253666-048US/Sep.2013)
vmovntdq	MOVNTDQ	Store Packed Integers Using Non-Temporal Hint	page 5-371 (319433-016/Oct. 2013)
vmovntdqa	MOVNTDQA	Load Double Quadword Non-Temporal Aligned Hint	page 5-369 (319433-016/Oct. 2013)
vmovntpd	MOVNTPD	Store Packed Double-Precision Floating-Point Values Using Non-Temporal Hint	page 5-373 (319433-016/Oct. 2013)
vmovntps	MOVNTPS	Store Packed Single-Precision Floating-Point Values Using Non-Temporal Hint	page 5-375 (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vmovq	MOVQ	Move Quadword	page 5-343 (319433-016/Oct. 2013)
vmovsd	MOVSD	Move or Merge Scalar Double-Precision Floating- Point Value	page 5-377 (319433-016/Oct. 2013)
vmovshdup	MOVSHDUP	Replicate Single FP Values	page 5-380 (319433-016/Oct. 2013)
vmovsldup	MOVSLDUP	Replicate Single FP Values	page 5-383 (319433-016/Oct. 2013)
vmovss	MOVSS	Move or Merge Scalar Single-Precision Floating- Point Value	page 5-386 (319433-016/Oct. 2013)
vmovupd	MOVUPD	Move Unaligned Packed Double-Precision Floating- Point Values	page 5-389 (319433-016/Oct. 2013)
vmovups	MOVUPS	Move Unaligned Packed Single-Precision Floating- Point Values	page 5-392 (319433-016/Oct. 2013)
vmpsadbw	MPSADBW	Compute Multiple Packed Sums of Absolute Difference	page 3-577 (253666-048US/ Sep.2013)
vmulpd	MULPD	Multiply Packed Double- Precision Floating-Point Values	page 5-395 (319433-016/Oct. 2013)
vmulps	MULPS	Multiply Packed Single- Precision Floating-Point Values	page 5-397 (319433-016/Oct. 2013)
vmulsd	MULSD	Multiply Scalar Double- Precision Floating-Point Value	page 5-400 (319433-016/Oct. 2013)
vmulss	MULSS	Multiply Scalar Single- Precision Floating-Point Values	page 5-402 (319433-016/Oct. 2013)
vorpd	ORPD	Bitwise Logical OR of Double-Precision Floating- Point Values	page 4-13 (253667-048US/ Sep.2013)
vorps	ORPS	Bitwise Logical OR of Single-Precision Floating- Point Values	page 4-15 (253667-048US/ Sep.2013)

3.6 AVX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vpabs(w b d)	PABSB PABSW PABSD PABSQ	Packed Absolute Value	page 5-404 (319433-016/Oct. 2013)
vpakss(dw wb)	PACKSSWB PACKSSDW	Pack with Signed Saturation	page 4-27 (253667-048US/ Sep.2013)
vpakusdw	PACKUSDW	Pack with Unsigned Saturation	page 4-32 (253667-048US/ Sep.2013)
vpakuswb	PACKUSWB	Pack with Unsigned Saturation	page 4-35 (253667-048US/ Sep.2013)
vpadd(q w b d)	PADDB PADDW PADDD PADDQ	Add Packed Integers	page 5-408 (319433-016/Oct. 2013)
vpadds(w b)	PADDSB PADDSW	Add Packed Signed Integers with Signed Saturation	page 4-44 (253667-048US/ Sep.2013)
vpaddus(w b)	PADDUSB PADDUSW	Add Packed Unsigned Integers with Unsigned Saturation	page 4-47 (253667-048US/ Sep.2013)
vpalignr	PALIGNR	Packed Align Right	page 4-50 (253667-048US/ Sep.2013)
vpand	PAND	Logical AND	page 5-413 (319433-016/Oct. 2013)
vpandn	PANDN	Logical AND NOT	page 5-416 (319433-016/Oct. 2013)
vpavg(w b)	PAVGB PAVGW	Average Packed Integers	page 4-58 (253667-048US/ Sep.2013)
vpblendvb	PBLENDVB	Variable Blend Packed Bytes	page 4-61 (253667-048US/ Sep.2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vblendw	PBLENDW	Blend Packed Words	page 4-65 (253667-048US/ Sep.2013)
vpcmpeq(q w b d)	PCMPEQB PCMPEQW PCMPEQD PCMPEQQ	Compare Packed Integers for Equality	page 5-419 (319433-016/Oct. 2013)
vcmpestri	PCMPESTRI	Packed Compare Explicit Length Strings, Return Index	page 4-77 (253667-048US/ Sep.2013)
vcmpestrm	PCMPESTRM	Packed Compare Explicit Length Strings, Return Mask	page 4-79 (253667-048US/ Sep.2013)
vpcmpgt(q w b d)	PCMPGTB PCMPGTW PCMPGTD PCMPGTQ	Compare Packed Integers for Greater Than	page 5-424 (319433-016/Oct. 2013)
vcmpistri	PCMPISTRI	Packed Compare Implicit Length Strings, Return Index	page 4-87 (253667-048US/ Sep.2013)
vcmpistrm	PCMPISTRM	Packed Compare Implicit Length Strings, Return Mask	page 4-89 (253667-048US/ Sep.2013)
vpextr(q b d)	PEXTRB PEXTRD PEXTRQ	Extract Byte/Dword/Qword	page 4-95 (253667-048US/ Sep.2013)
vpextrw	PEXTRW	Extract Word	page 4-98 (253667-048US/ Sep.2013)
vphaddsw	PHADDSW	Packed Horizontal Add and Saturate	page 4-105 (253667-048US/ Sep.2013)
vphadd(w d)	PHADDW PHADDD	Packed Horizontal Add	page 4-101 (253667-048US/ Sep.2013)
vphminposuw	PHMINPOSUW	Packed Horizontal Word Minimum	page 4-107 (253667-048US/ Sep.2013)

3.6 AVX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vphsubsw	PHSUBSW	Packed Horizontal Subtract and Saturate	page 4-112 (253667-048US/ Sep.2013)
vphsub(w d)	PHSUBW PHSUBD	Packed Horizontal Subtract	page 4-109 (253667-048US/ Sep.2013)
vpinsr(q b w d)	PINSRB PINSRD PINSRQ	Insert Byte/Dword/Qword	page 4-114 (253667-048US/ Sep.2013)
vpinsrw	PINSRW	Insert Word	page 4-116 (253667-048US/ Sep.2013)
vpmadubsw	PMADDUBSW	Multiply and Add Packed Signed and Unsigned Bytes	page 4-118 (253667-048US/ Sep.2013)
vpmadddw	PMADDWD	Multiply and Add Packed Integers	page 4-120 (253667-048US/ Sep.2013)
vpmaxs(w b d)	PMAXSB PMAXSW PMAXSD PMAXSQ	Maximum of Packed Signed Integers	page 5-471 (319433-016/Oct. 2013)
vpmaxub	PMAXUB	Maximum of Packed Unsigned Byte Integers	page 4-131 (253667-048US/ Sep.2013)
vpmaxud	PMAXUD PMAXUQ	Maximum of Packed Unsigned Integers	page 5-476 (319433-016/Oct. 2013)
vpmaxuw	PMAXUW	Maximum of Packed Word Integers	page 4-136 (253667-048US/ Sep.2013)
vpminsb	PMINSB	Minimum of Packed Signed Byte Integers	page 4-138 (253667-048US/ Sep.2013)
vpminsd	PMINSD PMINSQ	Minimum of Packed Signed Integers	page 5-479 (319433-016/Oct. 2013)
vpminsw	PMINSW	Minimum of Packed Signed Word Integers	page 4-143 (253667-048US/ Sep.2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vpm _{in} ub	PMINUB	Minimum of Packed Unsigned Byte Integers	page 4-146 (253667-048US/ Sep.2013)
vpm _{in} ud	PMINUD PMINUQ	Minimum of Packed Unsigned Integers	page 5-482 (319433-016/Oct. 2013)
vpm _{in} uw	PMINUW	Minimum of Packed Word Integers	page 4-151 (253667-048US/ Sep.2013)
vpmovmskb	PMOVMASK	Move Byte Mask	page 4-153 (253667-048US/ Sep.2013)
vpmovsx(bd bq bw dq wd wq)	PMOVXSX	Packed Move with Sign Extend	page 5-500 (319433-016/Oct. 2013)
vpmovzx(bd bq bw dq wd wq)	PMOVZSX	Packed Move with Zero Extend	page 5-507 (319433-016/Oct. 2013)
vpmul _{dq}	PMULDQ	Multiply Packed Doubleword Integers	page 5-514 (319433-016/Oct. 2013)
vpmul _{hrsw}	PMULHRSW	Packed Multiply High with Round and Scale	page 4-165 (253667-048US/ Sep.2013)
vpmul _{huw}	PMULHUW	Multiply Packed Unsigned Integers and Store High Result	page 4-168 (253667-048US/ Sep.2013)
vpmul _{hw}	PMULHW	Multiply Packed Signed Integers and Store High Result	page 4-172 (253667-048US/ Sep.2013)
vpmul _{lld}	PMULLD	Multiply Packed Integers and Store Low Result	page 5-516 (319433-016/Oct. 2013)
vpmul _{llw}	PMULLW	Multiply Packed Signed Integers and Store Low Result	page 4-177 (253667-048US/ Sep.2013)
vpmul _{udq}	PMULUDQ	Multiply Packed Unsigned Doubleword Integers	page 5-519 (319433-016/Oct. 2013)
vpor	POR	Bitwise Logical Or	page 5-521 (319433-016/Oct. 2013)

3.6 AVX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vpsadbw	PSADBW	Compute Sum of Absolute Differences	page 4-198 (253667-048US/ Sep.2013)
vpshufb	PSHUFB	Packed Shuffle Bytes	page 4-201 (253667-048US/ Sep.2013)
vpshufd	PSHUFD	Shuffle Packed Doublewords	page 5-533 (319433-016/Oct. 2013)
vpshufhw	PSHUFHW	Shuffle Packed High Words	page 4-206 (253667-048US/ Sep.2013)
vpshuflw	PSHUFLW	Shuffle Packed Low Words	page 4-208 (253667-048US/ Sep.2013)
vpsign(w b d)	PSIGNB PSIGNW PSIGND	Packed SIGN	page 4-211 (253667-048US/ Sep.2013)
vpslldq	PSLLDQ	Shift Double Quadword Left Logical	page 4-215 (253667-048US/ Sep.2013)
vpsll(q w d)	PSLLW PSLLD PSLLQ	Bit Shift Left	page 5-536 (319433-016/Oct. 2013)
vpsra(w d)	PSRAW	Bit Shift Arithmetic Right	page 5-544 (319433-016/Oct. 2013)
vpsrldq	PSRLDQ	Shift Double Quadword Right Logical	page 4-228 (253667-048US/ Sep.2013)
vpsrl(q w d)	PSRLW PSRLD PSRLQ	Shift Packed Data Right Logical	page 5-550 (319433-016/Oct. 2013)
vpsub(q w b d)	PSUBB PSUBW PSUBD PSUBQ	Packed Integer Subtract	page 5-563 (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vpsubs (w b)	PSUBSB PSUBSW	Subtract Packed Signed Integers with Signed Saturation	page 4-243 (253667-048US/ Sep.2013)
vpsubus (w b)	PSUBUSB PSUBUSW	Subtract Packed Unsigned Integers with Unsigned Saturation	page 4-246 (253667-048US/ Sep.2013)
vptest	PTEST	Logical Compare	page 4-249 (253667-048US/ Sep.2013)
vpunpckh (bw dq qdq wd)	PUNPCKHBW PUNPCKHWD PUNPCKHDQ PUNPCKHQDQ	Unpack High Data	page 5-571 (319433-016/Oct. 2013)
vpunpckl (bw dq qdq wd)	PUNPCKLBW PUNPCKLWD PUNPCKLDQ PUNPCKLQDQ	Unpack Low Data	page 5-578 (319433-016/Oct. 2013)
vpxor	PXOR PXORD PXORQ	Exclusive Or	page 5-612 (319433-016/Oct. 2013)
vrcpps	RCPPS	Compute Reciprocals of Packed Single-Precision Floating-Point Values	page 4-280 (253667-048US/ Sep.2013)
vrcpss	RCPSS	Compute Reciprocal of Scalar Single-Precision Floating-Point Values	page 4-282 (253667-048US/ Sep.2013)
vroundpd	ROUNDPD	Round Packed Double Precision Floating-Point Values	page 4-312 (253667-048US/ Sep.2013)
vroundps	ROUNDPS	Round Packed Single Precision Floating-Point Values	page 4-315 (253667-048US/ Sep.2013)
vroundsd	ROUNDSD	Round Scalar Double Precision Floating-Point Values	page 4-318 (253667-048US/ Sep.2013)
vroundss	ROUNDSS	Round Scalar Single Precision Floating-Point Values	page 4-320 (253667-048US/ Sep.2013)

3.6 AVX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vrsqrtps	RSQRTPS	Compute Reciprocals of Square Roots of Packed Single-Precision Floating-Point Values	page 4-324 (253667-048US/Sep.2013)
vrsqrtss	RSQRTSS	Compute Reciprocal of Square Root of Scalar Single-Precision Floating-Point Value	page 4-326 (253667-048US/Sep.2013)
vshufpd	SHUFPD	Shuffle Packed Double-Precision Floating-Point Values	page 5-589 (319433-016/Oct. 2013)
vshufps	SHUFPS	Shuffle Packed Single-Precision Floating-Point Values	page 5-593 (319433-016/Oct. 2013)
vsqrtpd	SQRTPD	Square Root of Double-Precision Floating-Point Values	page 5-597 (319433-016/Oct. 2013)
vsqrtps	SQRTPS	Square Root of Single-Precision Floating-Point Values	page 5-599 (319433-016/Oct. 2013)
vsqrtsd	SQRTPD	Compute Square Root of Scalar Double-Precision Floating-Point Value	page 5-601 (319433-016/Oct. 2013)
vsqrtss	SQRTPS	Compute Square Root of Scalar Single-Precision Value	page 5-603 (319433-016/Oct. 2013)
vstmxcsr	STMXCSR	Store MXCSR Register State	page 4-378 (253667-048US/Sep.2013)
vsubpd	SUBPD	Subtract Packed Double-Precision Floating-Point Values	page 5-656 (319433-016/Oct. 2013)
vsubps	SUBPS	Subtract Packed Single-Precision Floating-Point Values	page 5-659 (319433-016/Oct. 2013)
vsubsd	SUBSD	Subtract Scalar Double-Precision Floating-Point Value	page 5-662 (319433-016/Oct. 2013)
vsubss	SUBSS	Subtract Scalar Single-Precision Floating-Point Value	page 5-664 (319433-016/Oct. 2013)
vucomisd	UCOMISD	Unordered Compare Scalar Double-Precision Floating-	page 5-666 (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
		Point Values and Set EFLAGS	
<code>vucomiss</code>	UCOMISS	Unordered Compare Scalar Single-Precision Floating-Point Values and Set EFLAGS	page 5-668 (319433-016/Oct. 2013)
<code>vunpckhpd</code>	UNPCKHPD	Unpack and Interleave High Packed Double-Precision Floating-Point Values	page 5-670 (319433-016/Oct. 2013)
<code>vunpckhps</code>	UNPCKHPS	Unpack and Interleave High Packed Single-Precision Floating-Point Values	page 5-673 (319433-016/Oct. 2013)
<code>vunpcklpd</code>	UNPCKLPD	Unpack and Interleave Low Packed Double-Precision Floating-Point Values	page 5-677 (319433-016/Oct. 2013)
<code>vunpcklps</code>	UNPCKLPS	Unpack and Interleave Low Packed Single-Precision Floating-Point Values	page 5-680 (319433-016/Oct. 2013)
<code>vbroadcast(f128 sd ss)</code>	VBROADCAST	Load with Broadcast Floating-Point Data	page 5-27 (319433-016/Oct. 2013)
<code>vextractf128</code>	VEEXTRACTF128 VEEXTRACTF32x4 VEEXTRACTF64x4	Extract Packed Floating-Point Values	page 5-152 (319433-016/Oct. 2013)
<code>vinser tf128</code>	VINSERTF128 VINSERTF32x4 VINSERTF64x4	Insert Packed Floating-Point Values	page 5-305 (319433-016/Oct. 2013)
<code>vmaskmov(pd ps)</code>	VMASKMOV	Conditional SIMD Packed Loads and Stores	page 4-506 (253667-048US/Sep.2013)
<code>vperm2f128</code>	VPERM2F128	Permute Floating-Point Values	page 4-527 (253667-048US/Sep.2013)
<code>vpermilpd</code>	VPERMILPD	Permute Double-Precision Floating-Point Values	page 5-445 (319433-016/Oct. 2013)
<code>vpermilps</code>	VPERMILPS	Permute Single-Precision Floating-Point Values	page 5-450 (319433-016/Oct. 2013)

3.7 AVX2 Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vtestp(d s)	VTESTPDVTESTPS	Packed Bit Test	page 4-538 (253667-048US/ Sep.2013)
vzeroall	VZEROALL	Zero All YMM Registers	page 4-541 (253667-048US/ Sep.2013)
vzeroupper	VZERoupper	Zero Upper Bits of YMM Registers	page 4-543 (253667-048US/ Sep.2013)
vxorpd	XORPD	Bitwise Logical XOR for Double-Precision Floating-Point Values	page 4-572 (253667-048US/ Sep.2013)
vxorps	XORPS	Bitwise Logical XOR for Single-Precision Floating-Point Values	page 4-574 (253667-048US/ Sep.2013)
vpclmulqdq	PCLMULQDQ	Carry-Less Multiplication Quadword Requires PCLMULQDQ CPUID-flag	page 4-68 (253667-048US/ Sep.2013)

3.7 AVX2 Instructions

TABLE 3-24 AVX2 Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vmovntdqa	MOVNTDQA	Load Double Quadword Non-Temporal Aligned Hint	page 5-369 (319433-016/Oct. 2013)
vmpsadbw	MPSADBW	Compute Multiple Packed Sums of Absolute Difference	page 3-577 (253666-048US/ Sep.2013)
vpabs(w b d)	PABS PABS PABS PABS	Packed Absolute Value	page 5-404 (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vpackss(dw wb)	PACKSSWB PACKSSDW	Pack with Signed Saturation	page 4-27 (253667-048US/ Sep.2013)
vpackusdw	PACKUSDW	Pack with Unsigned Saturation	page 4-32 (253667-048US/ Sep.2013)
vpackuswb	PACKUSWB	Pack with Unsigned Saturation	page 4-35 (253667-048US/ Sep.2013)
vpadd(q w b d)	PADDB PADDW PADDD PADDQ	Add Packed Integers	page 5-408 (319433-016/Oct. 2013)
vpadds(w b)	PADDSB PADDSW	Add Packed Signed Integers with Signed Saturation	page 4-44 (253667-048US/ Sep.2013)
vpaddus(w b)	PADDUSB PADDUSW	Add Packed Unsigned Integers with Unsigned Saturation	page 4-47 (253667-048US/ Sep.2013)
vpsalignr	PALIGNR	Packed Align Right	page 4-50 (253667-048US/ Sep.2013)
vpand	PAND	Logical AND	page 5-413 (319433-016/Oct. 2013)
vpandn	PANDN	Logical AND NOT	page 5-416 (319433-016/Oct. 2013)
vpavg(w b)	PAVGB PAVGW	Average Packed Integers	page 4-58 (253667-048US/ Sep.2013)
vpblendvb	PBLENDVB	Variable Blend Packed Bytes	page 4-61 (253667-048US/ Sep.2013)
vpblendw	PBLENDW	Blend Packed Words	page 4-65 (253667-048US/ Sep.2013)

3.7 AVX2 Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vpcmpeq(q w b d)	PCMPEQB PCMPEQW PCMPEQD PCMPEQQ	Compare Packed Integers for Equality	page 5-419 (319433-016/Oct. 2013)
vpcmpgt(q w b d)	PCMPGTB PCMPGTW PCMPGTD PCMPGTQ	Compare Packed Integers for Greater Than	page 5-424 (319433-016/Oct. 2013)
vphaddsw	PHADDSW	Packed Horizontal Add and Saturate	page 4-105 (253667-048US/Sep.2013)
vphadd(w d)	PHADDW PHADDD	Packed Horizontal Add	page 4-101 (253667-048US/Sep.2013)
vphsubsw	PHSUBSW	Packed Horizontal Subtract and Saturate	page 4-112 (253667-048US/Sep.2013)
vphsub(w d)	PHSUBW PHSUBD	Packed Horizontal Subtract	page 4-109 (253667-048US/Sep.2013)
vpaddubsw	PMADDUBSW	Multiply and Add Packed Signed and Unsigned Bytes	page 4-118 (253667-048US/Sep.2013)
vpaddwd	PMADDWD	Multiply and Add Packed Integers	page 4-120 (253667-048US/Sep.2013)
vpmaxs(w b d)	PMAXSB PMAXSW PMAXSD PMAXSQ	Maximum of Packed Signed Integers	page 5-471 (319433-016/Oct. 2013)
vpmaxub	PMAXUB	Maximum of Packed Unsigned Byte Integers	page 4-131 (253667-048US/Sep.2013)
vpmaxud	PMAXUD PMAXUQ	Maximum of Packed Unsigned Integers	page 5-476 (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vpmaxuw	PMAXUW	Maximum of Packed Word Integers	page 4-136 (253667-048US/ Sep.2013)
vpminsb	PMINSB	Minimum of Packed Signed Byte Integers	page 4-138 (253667-048US/ Sep.2013)
vpminsd	PMINSB PMINSQ	Minimum of Packed Signed Integers	page 5-479 (319433-016/Oct. 2013)
vpminsw	PMINSW	Minimum of Packed Signed Word Integers	page 4-143 (253667-048US/ Sep.2013)
vpminub	PMINUB	Minimum of Packed Unsigned Byte Integers	page 4-146 (253667-048US/ Sep.2013)
vpminud	PMINUB PMINUQ	Minimum of Packed Unsigned Integers	page 5-482 (319433-016/Oct. 2013)
vpminuw	PMINUW	Minimum of Packed Word Integers	page 4-151 (253667-048US/ Sep.2013)
vpmovmskb	PMOVMASK	Move Byte Mask	page 4-153 (253667-048US/ Sep.2013)
vpmovsx (bd bq bw dq wd wq)	PMOVSSX	Packed Move with Sign Extend	page 5-500 (319433-016/Oct. 2013)
vpmovzx (bd bq bw dq wd wq)	PMOVZSX	Packed Move with Zero Extend	page 5-507 (319433-016/Oct. 2013)
vpmuldq	PMULDQ	Multiply Packed Doubleword Integers	page 5-514 (319433-016/Oct. 2013)
vpmulhrsw	PMULHRWSW	Packed Multiply High with Round and Scale	page 4-165 (253667-048US/ Sep.2013)
vpmulhuw	PMULHUW	Multiply Packed Unsigned Integers and Store High Result	page 4-168 (253667-048US/ Sep.2013)
vpmulhw	PMULHW	Multiply Packed Signed Integers	page 4-172 (253667-048US/ Sep.2013)

3.7 AVX2 Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
		and Store High Result	
vpmulld	PMULLD	Multiply Packed Integers and Store Low Result	page 5-516 (319433-016/Oct. 2013)
vpmullw	PMULLW	Multiply Packed Signed Integers and Store Low Result	page 4-177 (253667-048US/Sep.2013)
vpmuludq	PMULUDQ	Multiply Packed Unsigned Doubleword Integers	page 5-519 (319433-016/Oct. 2013)
vpor	POR	Bitwise Logical Or	page 5-521 (319433-016/Oct. 2013)
vpsadbw	PSADBW	Compute Sum of Absolute Differences	page 4-198 (253667-048US/Sep.2013)
vpshufb	PSHUFB	Packed Shuffle Bytes	page 4-201 (253667-048US/Sep.2013)
vpshufd	PSHUFD	Shuffle Packed Doublewords	page 5-533 (319433-016/Oct. 2013)
vpshufhw	PSHUFHW	Shuffle Packed High Words	page 4-206 (253667-048US/Sep.2013)
vpshuflw	PSHUFLLW	Shuffle Packed Low Words	page 4-208 (253667-048US/Sep.2013)
vpsign(w b d)	PSIGNB PSIGNW PSIGND	Packed SIGN	page 4-211 (253667-048US/Sep.2013)
vpslldq	PSLLDQ	Shift Double Quadword Left Logical	page 4-215 (253667-048US/Sep.2013)
vpsll(q w d)	PSLLW PSLLD PSLLQ	Bit Shift Left	page 5-536 (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vpsra(w d)	PSRAW PSRAD PSRAQ	Bit Shift Arithmetic Right	page 5-544 (319433-016/Oct. 2013)
vpsrldq	PSRLDQ	Shift Double Quadword Right Logical	page 4-228 (253667-048US/ Sep.2013)
vpsrl(q w d)	PSRLW PSRLD PSRLQ	Shift Packed Data Right Logical	page 5-550 (319433-016/Oct. 2013)
vpsub(q w b d)	PSUBB PSUBW PSUBD PSUBQ	Packed Integer Subtract	page 5-563 (319433-016/Oct. 2013)
vpsubs(w b)	PSUBSB PSUBSW	Subtract Packed Signed Integers with Signed Saturation	page 4-243 (253667-048US/ Sep.2013)
vpsubus(w b)	PSUBUSB PSUBUSW	Subtract Packed Unsigned Integers with Unsigned Saturation	page 4-246 (253667-048US/ Sep.2013)
vpunpckh(bw dq qdq wd)	PUNPCKHBW PUNPCKHWD PUNPCKHDQ PUNPCKHQDQ	Unpack High Data	page 5-571 (319433-016/Oct. 2013)
vpunpckl(bw dq qdq wd)	PUNPCKLBW PUNPCKLWD PUNPCKLDQ PUNPCKLQDQ	Unpack Low Data	page 5-578 (319433-016/Oct. 2013)
vpxor	PXOR PXORD PXORQ	Exclusive Or	page 5-612 (319433-016/Oct. 2013)

3.7 AVX2 Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vbroadcast(sd ss)	VBROADCAST	Load with Broadcast Floating-Point Data	page 5-27 (319433-016/Oct. 2013)
vextracti128	VEXTRACTI128 VEXTRACTI32x4 VEXTRACTI64x4	Extract packed Integer Values	page 5-155 (319433-016/Oct. 2013)
vgatherdp(d s)	VGATHERDPS VGATHERDPD	Gather Packed Single, Packed Double with Signed Dword	page 5-273 (319433-016/Oct. 2013)
vgatherqp(d s)	VGATHERQPS VGATHERQPD	Gather Packed Single, Packed Double with Signed Qword Indices	page 5-275 (319433-016/Oct. 2013)
vinerti128	VINSERTI128 VINSERTI32x4 VINSERTI64x4	Insert Packed Integer Values	page 5-308 (319433-016/Oct. 2013)
vpblendd	VPBLEND	Blend Packed Dwords	page 4-509 (253667-048US/Sep.2013)
vpbroadcast(q w b d)	VPBROADCAST	Load Integer and Broadcast	page 5-34 (319433-016/Oct. 2013)
vbroadcasti128	VPBROADCAST VPBROADCASTI128	Broadcast Integer Data	page 4-511 (253667-048US/Sep.2013)
vperm2i128	VPERM2I128	Permute Integer Values	page 4-519 (253667-048US/Sep.2013)
vpermd	VPERMD	Permute Packed Doublewords/Elements	page 5-437 (319433-016/Oct. 2013)
vpermpd	VPERMPD	Permute Double-Precision Floating-Point Elements	page 5-455 (319433-016/Oct. 2013)
vpermps	VPERMPS	Permute Single-Precision	page 5-458 (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
		Floating-Point Elements	
vpermq	VPERMQ	Qwords Element Permutation	page 5-460 (319433-016/Oct. 2013)
vpgatherdd	VPGATHERDD VPGATHERDQ	Gather Packed Dword, Packed Qword with Signed Dword Indices	page 5-467 (319433-016/Oct. 2013)
vpgatherdq	VPGATHERDD VPGATHERDQ	Gather Packed Dword, Packed Qword with Signed Dword Indices	page 5-467 (319433-016/Oct. 2013)
vpgatherqd	VPGATHERQD VPGATHERQQ	Gather Packed Dword, Packed Qword with Signed Qword Indices	page 5-469 (319433-016/Oct. 2013)
vpgatherqq	VPGATHERQD VPGATHERQQ	Gather Packed Dword, Packed Qword with Signed Qword Indices	page 5-469 (319433-016/Oct. 2013)
vpmaskmov (q d)	VPMASKMOV	Conditional SIMD Integer Packed Loads and Stores	page 4-529 (253667-048US/Sep.2013)
vpsllv (q d)	VPSLLW VPSLLVD VPSLLVQ	Variable Bit Shift Left Logical	page 5-557 (319433-016/Oct. 2013)
vpsravd	VPSRAVD VPSRAVQ	Variable Bit Shift Right Arithmetic	page 5-609 (319433-016/Oct. 2013)
vpsrlv (q d)	VPSRLW VPSRLVD VPSRLVQ	Variable Bit Shift Right Logical	page 5-560 (319433-016/Oct. 2013)

3.8 BMI1 Instructions

TABLE 3-25 BMI1 Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
andn	ANDN	Logical AND NOT	page 3-53 (253666-048US/Sep.2013)
bextr	BEXTR	Bit Field Extract	page 3-66 (253666-048US/Sep.2013)
bsli	BLSI	Extract Lowest Set Isolated Bit	page 3-75 (253666-048US/Sep.2013)
blsmk	BLSMSK	Get Mask Up to Lowest Set Bit	page 3-76 (253666-048US/Sep.2013)
blsr	BLSR	Reset Lowest Set Bit	page 3-77 (253666-048US/Sep.2013)
lzcnt(q l w)	LZCNT	Count the Number of Leading Zero Bits	page 3-476 (253666-048US/Sep.2013)
tzcnt	TZCNT	Count the Number of Trailing Zero Bits	page 4-408 (253667-048US/Sep.2013)

3.9 BMI2 Instructions

TABLE 3-26 BMI2 Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
bzhi	BZHI	Zero High Bits Starting with Specified Bit Position	page 3-93 (253666-048US/Sep.2013)
mulx	MULX	Unsigned Multiply Without Affecting Flags	page 3-593 (253666-048US/Sep.2013)
pdep	PDEP	Parallel Bits Deposit	page 4-91 (253667-048US/Sep.2013)
pext	PEXT	Parallel Bits Extract	page 4-93 (253667-048US/Sep.2013)
rorx	RORX	Rotate Right Logical Without Affecting Flags	page 4-311 (253667-048US/Sep.2013)
sarx	SARX SHLX	Shift Without Affecting Flags	page 4-335 (253667-048US/Sep.2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
	SHRX		
shlx	SARX SHLX SHRX	Shift Without Affecting Flags	page 4-335 (253667-048US/Sep.2013)
shrx	SARX SHLX SHRX	Shift Without Affecting Flags	page 4-335 (253667-048US/Sep.2013)

3.10 F16C Instructions

TABLE 3-27 F16C Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vcvtph2ps	VCVTPH2PS	Convert 16-bit FP values to Single-Precision FP values	page 5-93 (319433-016/Oct.2013)
vcvtps2ph	VCVTPS2PH	Convert Single-Precision FP value to 16-bit FP value	page 5-96 (319433-016/Oct.2013)

3.11 FMA Instructions

TABLE 3-28 FMA Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vmadd132pd	VFMADD132PD VFMADD213PD VFMADD231PD	Fused Multiply-Add of Packed Double-Precision Floating-Point Values	page 4-436
vmadd213pd	VFMADD132PD VFMADD213PD VFMADD231PD	Fused Multiply-Add of Packed Double-Precision Floating-Point Values	page 4-436

3.11 FMA Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vfmadd231pd	VFMADD132PD VFMADD213PD VFMADD231PD	Fused Multiply-Add of Packed Double-Precision Floating-Point Values	page 4-436
vfmadd132ps	VFMADD132PS VFMADD213PS VFMADD231PS	Fused Multiply-Add of Packed Single-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmadd213ps	VFMADD132PS VFMADD213PS VFMADD231PS	Fused Multiply-Add of Packed Single-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmadd231ps	VFMADD132PS VFMADD213PS VFMADD231PS	Fused Multiply-Add of Packed Single-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmadd132sd	VFMADD132SD VFMADD213SD VFMADD231SD	Fused Multiply-Add of Scalar Double-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmadd213sd	VFMADD132SD VFMADD213SD VFMADD231SD	Fused Multiply-Add of Scalar Double-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmadd231sd	VFMADD132SD VFMADD213SD VFMADD231SD	Fused Multiply-Add of Scalar Double-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmadd132ss	VFMADD132SS VFMADD213SS VFMADD231SS	Fused Multiply-Add of Scalar Single-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmadd213ss	VFMADD132SS VFMADD213SS VFMADD231SS	Fused Multiply-Add of Scalar Single-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmadd231ss	VFMADD132SS VFMADD213SS	Fused Multiply-Add of Scalar Single-Precision Floating-Point	page (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
	VFMADD231SS		
vmaddsub132pd	VFMADDSUB132PD VFMADDSUB213PD VFMADDSUB231PD	Fused Multiply-Alternating Add/Subtract of Packed	page (319433-016/Oct. 2013)
vmaddsub213pd	VFMADDSUB132PD VFMADDSUB213PD VFMADDSUB231PD	Fused Multiply-Alternating Add/Subtract of Packed	page (319433-016/Oct. 2013)
vmaddsub231pd	VFMADDSUB132PD VFMADDSUB213PD VFMADDSUB231PD	Fused Multiply-Alternating Add/Subtract of Packed	page (319433-016/Oct. 2013)
vmaddsub132ps	VFMADDSUB132PS VFMADDSUB213PS VFMADDSUB231PS	Fused Multiply-Alternating Add/Subtract of Packed	page (319433-016/Oct. 2013)
vmaddsub213ps	VFMADDSUB132PS VFMADDSUB213PS VFMADDSUB231PS	Fused Multiply-Alternating Add/Subtract of Packed	page (319433-016/Oct. 2013)
vmaddsub231ps	VFMADDSUB132PS VFMADDSUB213PS VFMADDSUB231PS	Fused Multiply-Alternating Add/Subtract of Packed	page (319433-016/Oct. 2013)
vfmsub132pd	VFMSUB132PD VFMSUB213PD VFMSUB231PD	Fused Multiply-Subtract of Packed Double-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmsub213pd	VFMSUB132PD VFMSUB213PD VFMSUB231PD	Fused Multiply-Subtract of Packed Double-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmsub231pd	VFMSUB132PD VFMSUB213PD VFMSUB231PD	Fused Multiply-Subtract of Packed Double-Precision Floating-Point	page (319433-016/Oct. 2013)

3.11 FMA Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vfmsub132ps	VFMSUB132PS VFMSUB213PS VFMSUB231PS	Fused Multiply-Subtract of Packed Single-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmsub213ps	VFMSUB132PS VFMSUB213PS VFMSUB231PS	Fused Multiply-Subtract of Packed Single-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmsub231ps	VFMSUB132PS VFMSUB213PS VFMSUB231PS	Fused Multiply-Subtract of Packed Single-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmsub132sd	VFMSUB132SD VFMSUB213SD VFMSUB231SD	Fused Multiply-Subtract of Scalar Double-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmsub213sd	VFMSUB132SD VFMSUB213SD VFMSUB231SD	Fused Multiply-Subtract of Scalar Double-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmsub231sd	VFMSUB132SD VFMSUB213SD VFMSUB231SD	Fused Multiply-Subtract of Scalar Double-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmsub132ss	VFMSUB132SS VFMSUB213SS VFMSUB231SS	Fused Multiply-Subtract of Scalar Single-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmsub213ss	VFMSUB132SS VFMSUB213SS VFMSUB231SS	Fused Multiply-Subtract of Scalar Single-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmsub231ss	VFMSUB132SS VFMSUB213SS VFMSUB231SS	Fused Multiply-Subtract of Scalar Single-Precision Floating-Point	page (319433-016/Oct. 2013)
vfmsubadd132pd	VFMSUBADD132PD VFMSUBADD213PD	Fused Multiply-Alternating Subtract/Add of Packed	page (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
	VFMSUBADD231PD		
vfmsubadd213pd	VFMSUBADD132PD VFMSUBADD213PD VFMSUBADD231PD	Fused Multiply-Alternating Subtract/Add of Packed	page (319433-016/Oct. 2013)
vfmsubadd231pd	VFMSUBADD132PD VFMSUBADD213PD VFMSUBADD231PD	Fused Multiply-Alternating Subtract/Add of Packed	page (319433-016/Oct. 2013)
vfmsubadd132ps	VFMSUBADD132PS VFMSUBADD213PS VFMSUBADD231PS	Fused Multiply-Alternating Subtract/Add of Packed	page (319433-016/Oct. 2013)
vfmsubadd213ps	VFMSUBADD132PS VFMSUBADD213PS VFMSUBADD231PS	Fused Multiply-Alternating Subtract/Add of Packed	page (319433-016/Oct. 2013)
vfmsubadd231ps	VFMSUBADD132PS VFMSUBADD213PS VFMSUBADD231PS	Fused Multiply-Alternating Subtract/Add of Packed	page (319433-016/Oct. 2013)
vfnmadd132pd	VFNMADD132PD VFNMADD213PD VFNMADD231PD	Fused Negative Multiply-Add of Packed Double-Precision	page (319433-016/Oct. 2013)
vfnmadd213pd	VFNMADD132PD VFNMADD213PD VFNMADD231PD	Fused Negative Multiply-Add of Packed Double-Precision	page (319433-016/Oct. 2013)
vfnmadd231pd	VFNMADD132PD VFNMADD213PD VFNMADD231PD	Fused Negative Multiply-Add of Packed Double-Precision	page (319433-016/Oct. 2013)
vfnmadd132ps	VFNMADD132PS VFNMADD213PS VFNMADD231PS	Fused Negative Multiply-Add of Packed Single-Precision	page (319433-016/Oct. 2013)

3.11 FMA Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vfnmadd213ps	VFNMADD132PS VFNMADD213PS VFNMADD231PS	Fused Negative Multiply-Add of Packed Single-Precision	page (319433-016/Oct. 2013)
vfnmadd231ps	VFNMADD132PS VFNMADD213PS VFNMADD231PS	Fused Negative Multiply-Add of Packed Single-Precision	page (319433-016/Oct. 2013)
vfnmadd132sd	VFNMADD132SD VFNMADD213SD VFNMADD231SD	Fused Negative Multiply-Add of Scalar Double-Precision	page (319433-016/Oct. 2013)
vfnmadd213sd	VFNMADD132SD VFNMADD213SD VFNMADD231SD	Fused Negative Multiply-Add of Scalar Double-Precision	page (319433-016/Oct. 2013)
vfnmadd231sd	VFNMADD132SD VFNMADD213SD VFNMADD231SD	Fused Negative Multiply-Add of Scalar Double-Precision	page (319433-016/Oct. 2013)
vfnmadd132ss	VFNMADD132SS VFNMADD213SS VFNMADD231SS	Fused Negative Multiply-Add o	page 5-255(319433-016/Oct.2013)
vfnmadd213ss	VFNMADD132SS VFNMADD213SS VFNMADD231SS	Fused Negative Multiply-Add o	page 5-255(319433-016/Oct.2013)
vfnmadd231ss	VFNMADD132SS VFNMADD213SS VFNMADD231SS	Fused Negative Multiply-Add o	page 5-255(319433-016/Oct.2013)
vfnmsub132pd	VFNMSUB132PD VFNMSUB213PD VFNMSUB231PD	Fused Negative Multiply-Subtract of Packed Double- Precision Floating-Point Values	page 4-478(253667-048US/Sep.2013)
vfnmsub213pd	VFNMSUB132PD VFNMSUB213PD	Fused Negative Multiply-Subtract of Packed	page 4-478(253667-048US/Sep.2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
	VFNMSUB231PD	Double- Precision Floating-Point Values	
vfnmsub231pd	VFNMSUB132PD VFNMSUB213PD VFNMSUB231PD	Fused Negative Multiply-Subtract of Packed Double- Precision Floating-Point Values	page 4-478(253667-048US/Sep.2013)
vfnmsub132ps	VFNMSUB132PS VFNMSUB213PS VFNMSUB231PS	Fused Negative Multiply-Subtract of Packed Single-Precision	page (319433-016/Oct. 2013)
vfnmsub213ps	VFNMSUB132PS VFNMSUB213PS VFNMSUB231PS	Fused Negative Multiply-Subtract of Packed Single-Precision	page (319433-016/Oct. 2013)
vfnmsub231ps	VFNMSUB132PS VFNMSUB213PS VFNMSUB231PS	Fused Negative Multiply-Subtract of Packed Single-Precision	page (319433-016/Oct. 2013)
vfnmsub132sd	VFNMSUB132SD VFNMSUB213SD VFNMSUB231SD	Fused Negative Multiply-Subtract of Scalar Double-Precision	page (319433-016/Oct. 2013)
vfnmsub213sd	VFNMSUB132SD VFNMSUB213SD VFNMSUB231SD	Fused Negative Multiply-Subtract of Scalar Double-Precision	page (319433-016/Oct. 2013)
vfnmsub231sd	VFNMSUB132SD VFNMSUB213SD VFNMSUB231SD	Fused Negative Multiply-Subtract of Scalar Double-Precision	page (319433-016/Oct. 2013)
vfnmsub132ss	VFNMSUB132SS VFNMSUB213SS VFNMSUB231SS	Fused Negative Multiply-Subtract of Scalar Single-Precision	page (319433-016/Oct. 2013)
vfnmsub213ss	VFNMSUB132SS VFNMSUB213SS VFNMSUB231SS	Fused Negative Multiply-Subtract of Scalar Single-Precision	page (319433-016/Oct. 2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vfnmsub231ss	VFNMSUB132SS VFNMSUB213SS VFNMSUB231SS	Fused Negative Multiply-Subtract of Scalar Single-Precision	page (319433-016/Oct. 2013)

3.12 FSGSBASE Instructions

TABLE 3-29 FSGSBASE Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
rdfsbase(l q)	RDFSBASE RDGSBASE	Read FS/GS Segment Base	page 4-284 (253667-048US/Sep.2013)
rdgsbase(l q)	RDFSBASE RDGSBASE	Read FS/GS Segment Base	page 4-284 (253667-048US/Sep.2013)
wrfsbase(l q)	WRFSBASE WRGSBASE	Write FS/GS Segment Base	page 4-548 (253667-048US/Sep.2013)
wrgsbase(l q)	WRFSBASE WRGSBASE	Write FS/GS Segment Base	page 4-548 (253667-048US/Sep.2013)

3.13 MMX Instructions

The MMX instructions enable x86 processors to perform single-instruction, multiple-data (SIMD) operations on packed byte, word, doubleword, or quadword integer operands contained in memory, in MMX registers, or in general-purpose registers.

3.13.1 Data Transfer Instructions (MMX)

The data transfer instructions move doubleword and quadword operands between MMX registers and between MMX registers and memory.

TABLE 3-30 Data Transfer Instructions (MMX)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
movd	MOVD	move doubleword	movdq valid only under -m64
movq	MOVQ	move quadword	valid only under -m64

3.13.2 Conversion Instructions (MMX)

The conversion instructions pack and unpack bytes, words, and doublewords.

TABLE 3-31 Conversion Instructions (MMX)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
packssdw	PACKSSDW	pack doublewords into words with signed saturation	
packsswb	PACKSSWB	pack words into bytes with signed saturation	
packuswb	PACKUSWB	pack words into bytes with unsigned saturation	
punpckhbw	PUNPCKHBW	unpack high-order bytes	
punpckhdq	PUNPCKHDQ	unpack high-order doublewords	
punpckhwd	PUNPCKHWD	unpack high-order words	
punpcklbw	PUNPCKLBW	unpack low-order bytes	
punpckldq	PUNPCKLDQ	unpack low-order doublewords	
punpcklwd	PUNPCKLWD	unpack low-order words	

3.13.3 Packed Arithmetic Instructions (MMX)

The packed arithmetic instructions perform packed integer arithmetic on packed byte, word, and doubleword integers.

TABLE 3-32 Packed Arithmetic Instructions (MMX)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
paddb	PADDB	add packed byte integers	
padd	PADD	add packed doubleword integers	
paddsb	PADDSB	add packed signed byte integers with signed saturation	
paddsw	PADDSW	add packed signed word integers with signed saturation	
paddusb	PADDUSB	add packed unsigned byte integers with unsigned saturation	
paddusw	PADDUSW	add packed unsigned word integers with unsigned saturation	
paddw	PADDW	add packed word integers	
pmaddwd	PMADDWD	multiply and add packed word integers	
pmulhw	PMULHW	multiply packed signed word integers and store high result	
pmullw	PMULLW	multiply packed signed word integers and store low result	
psubb	PSUBB	subtract packed byte integers	
psubd	PSUBD	subtract packed doubleword integers	
psubsb	PSUBSB	subtract packed signed byte integers with signed saturation	
psubsw	PSUBSW	subtract packed signed word integers with signed saturation	
psubusb	PSUBUSB	subtract packed unsigned byte integers with unsigned saturation	
psubusw	PSUBUSW	subtract packed unsigned word integers with unsigned saturation	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
psubw	PSUBW	subtract packed word integers	

3.13.4 Comparison Instructions (MMX)

The compare instructions compare packed bytes, words, or doublewords.

TABLE 3-33 Comparison Instructions (MMX)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
pcmpeqb	PCMPEQB	compare packed bytes for equal	
pcmpeqd	PCMPEQD	compare packed doublewords for equal	
pcmpeqw	PCMPEQW	compare packed words for equal	
pcmpgtb	PCMPGTB	compare packed signed byte integers for greater than	
pcmpgtd	PCMPGTD	compare packed signed doubleword integers for greater than	
pcmpgtw	PCMPGTW	compare packed signed word integers for greater than	

3.13.5 Logical Instructions (MMX)

The logical instructions perform logical operations on quadword operands.

TABLE 3-34 Logical Instructions (MMX)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
pand	PAND	bitwise logical AND	
pandn	PANDN	bitwise logical AND NOT	
por	POR	bitwise logical OR	
pxor	PXOR	bitwise logical XOR	

3.13.6 Shift and Rotate Instructions (MMX)

The shift and rotate instructions operate on packed bytes, words, doublewords, or quadwords in 64-bit operands.

TABLE 3-35 Shift and Rotate Instructions (MMX)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
pslld	PSLLD	shift packed doublewords left logical	
psllq	PSLLQ	shift packed quadword left logical	
psllw	PSLLW	shift packed words left logical	
psrad	PSRAD	shift packed doublewords right arithmetic	
psraw	PSRAW	shift packed words right arithmetic	
psrld	PSRLD	shift packed doublewords right logical	
psrlq	PSRLQ	shift packed quadword right logical	
psrlw	PSRLW	shift packed words right logical	

3.13.7 State Management Instructions (MMX)

The emms (EMMS) instruction clears the MMX state from the MMX registers.

TABLE 3-36 State Management Instructions (MMX)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
emms	EMMS	empty MMX state	

3.14 MOVBE Instructions

TABLE 3-37 MOVBE Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
movbe(q l w)	movbe	Reverse byte order in <source> and move to <destination>	325383-050US 3-519 Vol. 2A

3.15 PCLMULQDQ Instructions

TABLE 3-38 PCLMULQDQ Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
pclmulqdq	PCLMULQDQ	Carry-Less Multiplication Quadword	page 4-68 (253667-048US/ Sep.2013)

3.16 RDRAND Instructions

TABLE 3-39 RDRAND Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
rdrand(q l w)	RDRAND	Returns a random number	page 10-1 (319433-016/ Oct.2013)

3.17 SSE Instructions

SSE instructions are an extension of the SIMD execution model introduced with the MMX technology. SSE instructions are divided into four subgroups:

- SIMD single-precision floating-point instructions that operate on the XMM registers
- MXSCR state management instructions
- 64-bit SIMD integer instructions that operate on the MMX registers

- Instructions that provide cache control, prefetch, and instruction ordering functionality

3.17.1 SIMD Single-Precision Floating-Point Instructions (SSE)

The SSE SIMD instructions operate on packed and scalar single-precision floating-point values located in the XMM registers or memory.

3.17.1.1 Data Transfer Instructions (SSE)

The SSE data transfer instructions move packed and scalar single-precision floating-point operands between XMM registers and between XMM registers and memory.

TABLE 3-40 Data Transfer Instructions (SSE)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
movaps	MOVAPS	move four aligned packed single-precision floating-point values between XMM registers or memory	
movhlps	MOVHLPS	move two packed single-precision floating-point values from the high quadword of an XMM register to the low quadword of another XMM register	
movhps	MOVHPS	move two packed single-precision floating-point values to or from the high quadword of an XMM register or memory	
movlhps	MOVLHPS	move two packed single-precision floating-point values from the low quadword of an XMM register to the high quadword of another XMM register	
movlps	MOVLPS	move two packed single-precision floating-point values to or from the low quadword of an XMM register or memory	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
movmskps	MOVMSKPS	extract sign mask from four packed single-precision floating-point values	
movss	MOVSS	move scalar single-precision floating-point value between XMM registers or memory	
movups	MOVUPS	move four unaligned packed single-precision floating-point values between XMM registers or memory	

3.17.1.2 Packed Arithmetic Instructions (SSE)

SSE packed arithmetic instructions perform packed and scalar arithmetic operations on packed and scalar single-precision floating-point operands.

TABLE 3-41 Packed Arithmetic Instructions (SSE)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
addps	ADDPS	add packed single-precision floating-point values	
addss	ADDSS	add scalar single-precision floating-point values	
divps	DIVPS	divide packed single-precision floating-point values	
divss	DIVSS	divide scalar single-precision floating-point values	
maxps	MAXPS	return maximum packed single-precision floating-point values	
maxss	MAXSS	return maximum scalar single-precision floating-point values	
minps	MINPS	return minimum packed single-precision floating-point values	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
minss	MINSS	return minimum scalar single-precision floating-point values.	
mulps	MULPS	multiply packed single-precision floating-point values	
mulss	MULSS	multiply scalar single-precision floating-point values	
rcpps	RCPPS	compute reciprocals of packed single-precision floating-point values	
rcpss	RCPSS	compute reciprocal of scalar single-precision floating-point values	
rsqrtps	RSQRTPS	compute reciprocals of square roots of packed single-precision floating-point values	
rsqrtss	RSQRTSS	compute reciprocal of square root of scalar single-precision floating-point values	
sqrtps	SQRTPS	compute square roots of packed single-precision floating-point values	
sqrtss	SQRTSS	compute square root of scalar single-precision floating-point values	
subps	SUBPS	subtract packed single-precision floating-point values	
subss	SUBSS	subtract scalar single-precision floating-point values	

3.17.1.3 Comparison Instructions (SSE)

The SSE compare instructions compare packed and scalar single-precision floating-point operands.

TABLE 3-42 Comparison Instructions (SSE)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
cmpps	CMPPS	compare packed single-precision floating-point values	
cmpss	CMPS	compare scalar single-precision floating-point values	
comiss	COMISS	perform ordered comparison of scalar single-precision floating-point values and set flags in EFLAGS register	
ucomiss	UCOMISS	perform unordered comparison of scalar single-precision floating-point values and set flags in EFLAGS register	

3.17.1.4 Logical Instructions (SSE)

The SSE logical instructions perform bitwise AND, AND NOT, OR, and XOR operations on packed single-precision floating-point operands.

TABLE 3-43 Logical Instructions (SSE)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
andnps	ANDNPS	perform bitwise logical AND NOT of packed single-precision floating-point values	
andps	ANDPS	perform bitwise logical AND of packed single-precision floating-point values	
orps	ORPS	perform bitwise logical OR of packed single-precision floating-point values	
xorps	XORPS	perform bitwise logical XOR of packed single-precision floating-point values	

3.17.1.5 Shuffle and Unpack Instructions (SSE)

The SSE shuffle and unpack instructions shuffle or interleave single-precision floating-point values in packed single-precision floating-point operands.

TABLE 3-44 Shuffle and Unpack Instructions (SSE)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
shufps	SHUFPS	shuffles values in packed single-precision floating-point operands	
unpckhps	UNPCKHPS	unpacks and interleaves the two high-order values from two single-precision floating-point operands	
unpcklps	UNPCKLPS	unpacks and interleaves the two low-order values from two single-precision floating-point operands	

3.17.1.6 Conversion Instructions (SSE)

The SSE conversion instructions convert packed and individual doubleword integers into packed and scalar single-precision floating-point values.

TABLE 3-45 Conversion Instructions (SSE)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
cvtpi2ps	CVTPI2PS	convert packed doubleword integers to packed single-precision floating-point values	
cvtps2pi	CVTPS2PI	convert packed single-precision floating-point values to packed doubleword integers	
cvtsi2ss	CVTSI2SS	convert doubleword integer to scalar single-precision floating-point value	
cvts2si	CVTS2SI	convert scalar single-precision floating-point value to a doubleword integer	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
cvttps2pi	CVTTPS2PI	convert with truncation packed single-precision floating-point values to packed doubleword integers	
cvttss2si	CVTTSS2SI	convert with truncation scalar single-precision floating-point value to scalar doubleword integer	

3.17.2 MXCSR State Management Instructions (SSE)

The MXCSR state management instructions save and restore the state of the MXCSR control and status register.

TABLE 3-46 MXCSR State Management Instructions (SSE)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
ldmxcsr	LDMXCSR	load %mxcsr register	
stmxcsr	STMXCSR	save %mxcsr register state	

3.17.3 64–Bit SIMD Integer Instructions (SSE)

The SSE 64–bit SIMD integer instructions perform operations on packed bytes, words, or doublewords in MMX registers.

TABLE 3-47 64–Bit SIMD Integer Instructions (SSE)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
pavgb	PAVGB	compute average of packed unsigned byte integers	
pavgw	PAVGW	compute average of packed unsigned word integers	
peextrw	PEXTRW	extract word	
pinsrw	PINSRW	insert word	
pmaxsw	PMAXSW	maximum of packed signed word integers	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
pmaxub	PMAXUB	maximum of packed unsigned byte integers	
pminsw	PMINSW	minimum of packed signed word integers	
pminub	PMINUB	minimum of packed unsigned byte integers	
pmovmskb	PMOVMASKB	move byte mask	
pmulhuw	PMULHUW	multiply packed unsigned integers and store high result	
psadbw	PSADBW	compute sum of absolute differences	
pshufw	PSHUFW	shuffle packed integer word in MMX register	

3.17.4 Miscellaneous Instructions (SSE)

The following instructions control caching, prefetching, and instruction ordering.

TABLE 3-48 Miscellaneous Instructions (SSE)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
maskmovq	MASKMOVQ	non-temporal store of selected bytes from an MMX register into memory	
movntps	MOVNTPS	non-temporal store of four packed single-precision floating-point values from an XMM register into memory	
movntq	MOVNTQ	non-temporal store of quadword from an MMX register into memory	
prefetchnta	PREFETCHNTA	prefetch data into non-temporal cache structure and into a location close to the processor	
prefetcht0	PREFETCHT0	prefetch data into all levels of the cache hierarchy	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
prefetcht1	PREFETCHT1	prefetch data into level 2 cache and higher	
prefetcht2	PREFETCHT2	prefetch data into level 2 cache and higher	
sfence	SFENCE	serialize store operations	

3.18 SSE2 Instructions

SSE2 instructions are an extension of the SIMD execution model introduced with the MMX technology and the SSE extensions. SSE2 instructions are divided into four subgroups:

- Packed and scalar double-precision floating-point instructions
- Packed single-precision floating-point conversion instructions
- 128-bit SIMD integer instructions
- Instructions that provide cache control and instruction ordering functionality

3.18.1 SSE2 Packed and Scalar Double-Precision Floating-Point Instructions

The SSE2 packed and scalar double-precision floating-point instructions operate on double-precision floating-point operands.

3.18.1.1 SSE2 Data Movement Instructions

The SSE2 data movement instructions move double-precision floating-point data between XMM registers and memory.

TABLE 3-49 SSE2 Data Movement Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
movapd	MOVAPD	move two aligned packed double-precision floating-point values between XMM registers and memory	
movhpd	MOVHPD	move high packed double-precision floating-point	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
		value to or from the high quadword of an XMM register and memory	
movlpd	MOVLPD	move low packed single-precision floating-point value to or from the low quadword of an XMM register and memory	
movmskpd	MOVMSKPD	extract sign mask from two packed double-precision floating-point values	
movsd	MOVSD	move scalar double-precision floating-point value between XMM registers and memory.	
movupd	MOVUPD	move two unaligned packed double-precision floating-point values between XMM registers and memory	

3.18.1.2 SSE2 Packed Arithmetic Instructions

The SSE2 arithmetic instructions operate on packed and scalar double-precision floating-point operands.

TABLE 3-50 SSE2 Packed Arithmetic Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
addpd	ADDPD	add packed double-precision floating-point values	
addsd	ADDSD	add scalar double-precision floating-point values	
divpd	DIVPD	divide packed double-precision floating-point values	
divsd	DIVSD	divide scalar double-precision floating-point values	
maxpd	MAXPD	return maximum packed double-precision floating-point values	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
maxsd	MAXSD	return maximum scalar double-precision floating-point value	
minpd	MINPD	return minimum packed double-precision floating-point values	
minsd	MINSD	return minimum scalar double-precision floating-point value	
mulpd	MULPD	multiply packed double-precision floating-point values	
mulsd	MULSD	multiply scalar double-precision floating-point values	
sqrtpd	SQRTPD	compute packed square roots of packed double-precision floating-point values	
sqrtsd	SQRSD	compute scalar square root of scalar double-precision floating-point value	
subpd	SUBPD	subtract packed double-precision floating-point values	
subsd	SUBSD	subtract scalar double-precision floating-point values	

3.18.1.3 SSE2 Logical Instructions

The SSE2 logical instructions operate on packed double-precision floating-point values.

TABLE 3-51 SSE2 Logical Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
andnpd	ANDNPD	perform bitwise logical AND NOT of packed double-precision floating-point values	
andpd	ANDPD	perform bitwise logical AND of packed double-	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
		precision floating-point values	
orpd	ORPD	perform bitwise logical OR of packed double-precision floating-point values	
xorpd	XORPD	perform bitwise logical XOR of packed double-precision floating-point values	

3.18.1.4 SSE2 Compare Instructions

The SSE2 compare instructions compare packed and scalar double-precision floating-point values and return the results of the comparison to either the destination operand or to the EFLAGS register.

TABLE 3-52 SSE2 Compare Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
cmpdp	CMPPD	compare packed double-precision floating-point values	
cmpsd	CMPSD	compare scalar double-precision floating-point values	
comisd	COMISD	perform ordered comparison of scalar double-precision floating-point values and set flags in EFLAGS register	
ucomisd	UCOMISD	perform unordered comparison of scalar double-precision floating-point values and set flags in EFLAGS register	

3.18.1.5 SSE2 Shuffle and Unpack Instructions

The SSE2 shuffle and unpack instructions operate on packed double-precision floating-point operands.

TABLE 3-53 SSE2 Shuffle and Unpack Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
shufpd	SHUFPD	shuffle values in packed double-precision floating-point operands	
unpckhpd	UNPCKHPD	unpack and interleave the high values from two packed double-precision floating-point operands	
unpcklpd	UNPCKLPD	unpack and interleave the low values from two packed double-precision floating-point operands	

3.18.1.6 SSE2 Conversion Instructions

The SSE2 conversion instructions convert packed and individual doubleword integers into packed and scalar double-precision floating-point values (and vice versa). These instructions also convert between packed and scalar single-precision and double-precision floating-point values.

TABLE 3-54 SSE2 Conversion Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
cvtdq2pd	CVTDQ2PD	convert packed doubleword integers to packed double-precision floating-point values	
cvtpd2dq	CVTPD2DQ	convert packed double-precision floating-point values to packed doubleword integers	
cvtpd2pi	CVTPD2PI	convert packed double-precision floating-point values to packed doubleword integers	
cvtpd2ps	CVTPD2PS	convert packed double-precision floating-point values to packed single-precision floating-point values	
cvtpi2pd	CVTPI2PD	convert packed doubleword integers to packed double-precision floating-point values	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
cvtps2pd	CVTPS2PD	convert packed single-precision floating-point values to packed double-precision floating-point values	
cvtsd2si	CVTSD2SI	convert scalar double-precision floating-point values to a doubleword integer	
cvtsd2ss	CVTSD2SS	convert scalar double-precision floating-point values to scalar single-precision floating-point values	
cvtsi2sd	CVTSI2SD	convert doubleword integer to scalar double-precision floating-point value	
cvts2sd	CVTS2SD	convert scalar single-precision floating-point values to scalar double-precision floating-point values	
cvttpd2dq	CVTTPD2DQ	convert with truncation packed double-precision floating-point values to packed doubleword integers	
cvttpd2pi	CVTTPD2PI	convert with truncation packed double-precision floating-point values to packed doubleword integers	
cvtt2sd2si	CVTTSD2SI	convert with truncation scalar double-precision floating-point values to scalar doubleword integers	

3.18.2 SSE2 Packed Single-Precision Floating-Point Instructions

The SSE2 packed single-precision floating-point instructions operate on single-precision floating-point and integer operands.

TABLE 3-55 SSE2 Packed Single-Precision Floating-Point Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
cvtdq2ps	CVTDQ2PS	convert packed doubleword integers to packed single-precision floating-point values	
cvtps2dq	CVTPS2DQ	convert packed single-precision floating-point values to packed doubleword integers	
cvttps2dq	CVTTPS2DQ	convert with truncation packed single-precision floating-point values to packed doubleword integers	

3.18.3 SSE2 128–Bit SIMD Integer Instructions

The SSE2 SIMD integer instructions operate on packed words, doublewords, and quadwords contained in XMM and MMX registers.

TABLE 3-56 SSE2 128–Bit SIMD Integer Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
movdq2q	MOVDQ2Q	move quadword integer from XMM to MMX registers	
movdqa	MOVDQA	move aligned double quadword	
movdqu	MOVDQU	move unaligned double quadword	
movq2dq	MOVQ2DQ	move quadword integer from MMX to XMM registers	
paddq	PADDQ	add packed quadword integers	
pmuludq	PMULUDQ	multiply packed unsigned doubleword integers	
pshufd	PSHUFQ	shuffle packed doublewords	
pshufhw	PSHUFHW	shuffle packed high words	
pshufw	PSHUFQ	shuffle packed low words	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
pslldq	PSLLDQ	shift double quadword left logical	
psrldq	PSRLDQ	shift double quadword right logical	
psubq	PSUBQ	subtract packed quadword integers	
punpckhqdq	PUNPCKHQDQ	unpack high quadwords	
punpcklqdq	PUNPCKLQDQ	unpack low quadwords	

3.18.4 SSE2 Miscellaneous Instructions

The SSE2 instructions described below provide additional functionality for caching non-temporal data when storing data from XMM registers to memory, and provide additional control of instruction ordering on store operations.

TABLE 3-57 SSE2 Miscellaneous Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
clflush	CLFLUSH	flushes and invalidates a memory operand and its associated cache line from all levels of the processor's cache hierarchy	
lfence	LFENCE	serializes load operations	
maskmovdqu	MASKMOVDQU	non-temporal store of selected bytes from an XMM register into memory	
mfence	MFENCE	serializes load and store operations	
movntdq	MOVNTDQ	non-temporal store of double quadword from an XMM register into memory	
movnti	MOVNTI	non-temporal store of a doubleword from a general-purpose register into memory	movntiq valid only under -m64
movntpd	MOVNTPD	non-temporal store of two packed double-precision	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
		floating-point values from an XMM register into memory	
pause	PAUSE	improves the performance of spin-wait loops	

3.19 SSE3 Instructions

TABLE 3-58 SSE3 Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
addsubpd	ADDSUBPD	Packed Double-FP Add/Subtract	page 3-35 (253666-048US/Sep.2013)
addsubps	ADDSUBPS	Packed Single-FP Add/Subtract	page 3-37 (253666-048US/Sep.2013)
haddpd	HADDPD	Packed Double-FP Horizontal Add	page 3-370 (253666-048US/Sep.2013)
haddps	HADDPs	Packed Single-FP Horizontal Add	page 3-373 (253666-048US/Sep.2013)
hsubpd	HSUBPD	Packed Double-FP Horizontal Subtract	page 3-377 (253666-048US/Sep.2013)
hsubps	HSUBPS	Packed Single-FP Horizontal Subtract	page 3-380 (253666-048US/Sep.2013)
lddqu	LDDQU	Load Unaligned Integer 128 Bits	page 3-444 (253666-048US/Sep.2013)
movddup	MOVDDUP	Replicate Double FP Values	page 5-346 (319433-016/Oct.2013)
movshdup	MOVSHDUP	Replicate Single FP Values	page 5-380 (319433-016/Oct.2013)
movsldup	MOVSLDUP	Replicate Single FP Values	page 5-383 (319433-016/Oct.2013)

3.20 SSE4a Instructions

TABLE 3-59 SSE4a Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
extrq	EXTRQ		page 139 (AMD:26568-Rev.3.18-Oct.2013)
insertq	INSERTQ		page 154 (AMD:26568-Rev.3.18-Oct.2013)
movntsd	MOVNTSD		page 218 (AMD:26568-Rev.3.18-Oct.2013)
movntss	MOVNTSS		page 220 (AMD:26568-Rev.3.18-Oct.2013)

3.21 SSE4.1 Instructions

TABLE 3-60 SSE4.1 Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
blendpd	BLENDDPD	Blend Packed Double Precision Floating-Point Values	page 3-64 (253666-048US/Sep.2013)
blendps	BLENDPS	Blend Packed Single Precision Floating-Point Values	page 3-68 (253666-048US/Sep.2013)
blendvpd	BLENDVPD	Variable Blend Packed Double Precision Floating-Point Values	page 3-70 (253666-048US/Sep.2013)
blendvps	BLENDVPS	Variable Blend Packed Single Precision Floating-Point Values	page 3-72 (253666-048US/Sep.2013)
dppd	DPPD	Dot Product of Packed Double Precision Floating-Point Values	page 3-240 (253666-048US/Sep.2013)
dpps	DPPS	Dot Product of Packed Single Precision Floating-Point Values	page 3-242 (253666-048US/Sep.2013)
extractps	EXTRACTPS	Extract Packed Floating-Point Values	page 5-158 (319433-016/Oct.2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
insertps	INSERTPS	Insert Scalar Single-Precision Floating-Point Value	page 5-311 (319433-016/Oct.2013)
movntdqa	MOVNTDQA	Load Double Quadword Non-Temporal Aligned Hint	page 5-369 (319433-016/Oct.2013)
mpsadbw	MPSADBW	Compute Multiple Packed Sums of Absolute Difference	page 3-577 (253666-048US/Sep.2013)
packusdw	PACKUSDW	Pack with Unsigned Saturation	page 4-32 (253667-048US/Sep.2013)
pblendvb	PBLENDVB	Variable Blend Packed Bytes	page 4-61 (253667-048US/Sep.2013)
pblendw	PBLENDW	Blend Packed Words	page 4-65 (253667-048US/Sep.2013)
pcmpqq	PCMPQB PCMPQW PCMPQD PCMPQQ	Compare Packed Integers for Equality	page 5-419 (319433-016/Oct.2013)
peextr(q b d)	PEXTRB PEXTRD PEXTRQ	Extract Byte/Dword/Qword	page 4-95 (253667-048US/Sep.2013)
peextrw	PEXTRW	Extract Word	page 4-98 (253667-048US/Sep.2013)
phminposuw	PHMINPOSUW	Packed Horizontal Word Minimum	page 4-107 (253667-048US/Sep.2013)
pinsr(q b d)	PINSRB PINSRD PINSRQ	Insert Byte/Dword/Qword	page 4-114 (253667-048US/Sep.2013)
pmaxs(b d)	PMAXSB PMAXSW PMAXSD PMAXSQ	Maximum of Packed Signed Integers	page 5-471 (319433-016/Oct.2013)
pmaxud	PMAXUD	Maximum of Packed Unsigned Integers	page 5-476 (319433-016/Oct.2013)

3.21 SSE4.1 Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
	PMAXUQ		
pmaxuw	PMAXUW	Maximum of Packed Word Integers	page 4-136 (253667-048US/Sep.2013)
pminsb	PMINSB	Minimum of Packed Signed Byte Integers	page 4-138 (253667-048US/Sep.2013)
pminsd	PMINSD PMINSQ	Minimum of Packed Signed Integers	page 5-479 (319433-016/Oct.2013)
pminud	PMINUD PMINUQ	Minimum of Packed Unsigned Integers	page 5-482 (319433-016/Oct.2013)
pminuw	PMINUW	Minimum of Packed Word Integers	page 4-151 (253667-048US/Sep.2013)
pmovsx (bd bq bw dq wd wq)	PMOVSX	Packed Move with Sign Extend	page 5-500 (319433-016/Oct.2013)
pmovzx (bd bq bw dq wd wq)	PMOVZX	Packed Move with Zero Extend	page 5-507 (319433-016/Oct.2013)
pmuldq	PMULDQ	Multiply Packed Doubleword Integers	page 5-514 (319433-016/Oct.2013)
pmulld	PMULLD	Multiply Packed Integers and Store Low Result	page 5-516 (319433-016/Oct.2013)
pptest	PTEST	Logical Compare	page 4-249 (253667-048US/Sep.2013)
roundpd	ROUNDPD	Round Packed Double Precision Floating-Point Values	page 4-312 (253667-048US/Sep.2013)
roundps	ROUNDPS	Round Packed Single Precision Floating-Point Values	page 4-315 (253667-048US/Sep.2013)
roundsd	ROUNDSD	Round Scalar Double Precision Floating-Point Values	page 4-318 (253667-048US/Sep.2013)
roundss	ROUNDSS	Round Scalar Single Precision Floating-Point Values	page 4-320 (253667-048US/Sep.2013)

3.22 SSE4.2 Instructions

TABLE 3-61 SSE4.2 Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
pcmpestri	PCMPESTRI	Packed Compare Explicit Length Strings, Return Index	page 4-77 (253667-048US/Sep.2013)
pcmpestrm	PCMPESTRM	Packed Compare Explicit Length Strings, Return Mask	page 4-79 (253667-048US/Sep.2013)
pcmpgtq	PCMPGTB	Compare Packed Integers for Greater Than	page 5-424 (319433-016/Oct.2013)
pcmpistri	PCMPISTRI	Packed Compare Implicit Length Strings, Return Index	page 4-87 (253667-048US/Sep.2013)
pcmpistrm	PCMPISTRM	Packed Compare Implicit Length Strings, Return Mask	page 4-89 (253667-048US/Sep.2013)

3.23 SSSE3 Instructions

TABLE 3-62 SSSE3 Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
pabs(w b d)	PABSB PABSW PABSD PABSQ	Packed Absolute Value	page 5-404 (319433-016/Oct.2013)
paligr	PALIGNR	Packed Align Right	page 4-50 (253667-048US/Sep.2013)
phaddsw	PHADDSW	Packed Horizontal Add and Saturate	page 4-105 (253667-048US/Sep.2013)
phadd(w d)	PHADDW PHADDD	Packed Horizontal Add	page 4-101 (253667-048US/Sep.2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
pshsubsw	PHSUBSW	Packed Horizontal Subtract and Saturate	page 4-112 (253667-048US/Sep.2013)
pshsub(w d)	PHSUBW PHSUBD	Packed Horizontal Subtract	page 4-109 (253667-048US/Sep.2013)
pmaddubsw	PMADDUBSW	Multiply and Add Packed Signed and Unsigned Bytes	page 4-118 (253667-048US/Sep.2013)
pmulhrsw	PMULHRSW	Packed Multiply High with Round and Scale	page 4-165 (253667-048US/Sep.2013)
pshufb	PSHUFB	Packed Shuffle Bytes	page 4-201 (253667-048US/Sep.2013)
psign(w b d)	PSIGNB PSIGNW PSIGND	Packed SIGN	page 4-211 (253667-048US/Sep.2013)

3.24 Transactional Synchronization Extensions

TABLE 3-63 HLE Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
xtest	XTEST	Test If In Transactional Execution	page 4-588 (253667-048US/Sep.2013)

TABLE 3-64 RTM Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
xabort	XABORT	Transactional Abort	page 4-555 (253667-048US/Sep.2013)
xbegin(l w)	XBEGIN	Transactional Begin	page 4-559 (253667-048US/Sep.2013)
xend	XEND	Transactional End	page 4-564 (253667-048US/Sep.2013)
xtest	XTEST	Test If In Transactional Execution	page 4-588 (253667-048US/Sep.2013)

3.25 Operating System Support Instructions

The operating system support instructions provide functionality for process management, performance monitoring, debugging, and other systems tasks.

TABLE 3-65 Operating System Support Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
arpl	ARPL	adjust requested privilege level	
clts	CLTS	clear the task-switched flag	
hlt	HLT	halt processor	
invd	INVD	invalidate cache, no writeback	
invlpg	INVLPG	invalidate TLB entry	
lar	LAR	load access rights	larq valid only under -m64
lgdt	LGDT	load global descriptor table (GDT) register	
lidt	LIDT	load interrupt descriptor table (IDT) register	
lldt	LLDT	load local descriptor table (LDT) register	
lmsw	LMSW	load machine status word	
lock	LOCK	lock bus	
lsl	LSL	load segment limit	lslq valid only under -m64
ltr	LTR	load task register	
rdmsr	RDMSR	read model-specific register	
rdpmc	RDPMC	read performance monitoring counters	
rdtsc	RDTSC	read time stamp counter	
rsm	RSM	return from system management mode (SMM)	
sgdt	SGDT	store global descriptor table (GDT) register	
sidt	SIDT	store interrupt descriptor table (IDT) register	

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Notes
sldt	SLDT	store local descriptor table (LDT) register	sldtq valid only under -m64
smsw	SMSW	store machine status word	smswq valid only under -m64
str	STR	store task register	strq valid only under -m64
sysenter	SYSENTER	fast system call, transfers to a flat protected mode kernel at CPL=0	
sysexit	SYSEXIT	fast system call, transfers to a flat protected mode kernel at CPL=3	
verr	VERR	verify segment for reading	
verw	VERW	verify segment for writing	
wbinvd	WBINVD	invalidate cache, with writeback	
wrmsr	WRMSR	write model-specific register	

3.26 VMX Instructions

TABLE 3-66 VMX Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
invept	INVEPT	Invalidate Translations Derived from EPT	page 30-3 (326019-048US/Sep.2013)
invvpid	INVVPID	Invalidate Translations Based on VPID	page 30-6 (326019-048US/Sep.2013)
vmcall	VMCALL	Call to VM Monitor	page 30-9 (326019-048US/Sep.2013)
vmclear	VMCLEAR	Clear Virtual-Machine Control Structure	page 30-11 (326019-048US/Sep.2013)
vmfunc	VMFUNC	Invoke VM function	page 30-13 (326019-048US/Sep.2013)
vmlaunch	VMLAUNCH VMRESUME	Launch/Resume Virtual Machine	page 30-14 (326019-048US/Sep.2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
vmresume	VMLAUNCH VMRESUME	Launch/Resume Virtual Machine	page 30-14 (326019-048US/Sep.2013)
vmptfld	VMPTRLD	Load Pointer to Virtual-Machine Control Structure	page 30-17 (326019-048US/Sep.2013)
vmptrst	VMPTRST	Store Pointer to Virtual-Machine Control Structure	page 30-19 (326019-048US/Sep.2013)
vmread	VMREAD	Read Field from Virtual-Machine Control Structure	page 30-21 (326019-048US/Sep.2013)
vmwrite	VMWRITE	Write Field to Virtual-Machine Control Structure	page 0-24 (326019-048US/Sep.2013)
vmxoff	VMXOFF	Leave VMX Operation	page 30-27 (326019-048US/Sep.2013)
vmxon	VMXON	Enter VMX Operation	page 30-29 (326019-048US/Sep.2013)

3.27 XSAVE Instructions

TABLE 3-67 XSAVE Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
xsaveopt(64)	XSAVEOPT	Save Processor Extended States Optimized	page 4-583 (253667-048US/Sep.2013)

3.28 3DNow Instructions

TABLE 3-68 3DNow Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
femms	FEMMS		page 18 (AMD:26569-Rev.3.13-May.2013)
pavgusb	PAVGUSB		page 70 (AMD:26569-Rev.3.13-May.2013)
pf2id	PF2ID		page 88 (AMD:26569-Rev.3.13-May.2013)

3.28 3DNow Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
pf2iw	PF2IW		page 90 (AMD:26569-Rev.3.13-May.2013)
pfacc	PFACC		page 92 (AMD:26569-Rev.3.13-May.2013)
pfadd	PFADD		page 94 (AMD:26569-Rev.3.13-May.2013)
pfcmpeq	PFCMPEQ		page 96 (AMD:26569-Rev.3.13-May.2013)
pfcmpge	PFCMPGE		page 98 (AMD:26569-Rev.3.13-May.2013)
pfcmpgt	PFCMPGT		page 101 (AMD:26569-Rev.3.13-May.2013)
pfmax	PFMAX		page 103 (AMD:26569-Rev.3.13-May.2013)
pfmin	PFCMPGT		page 105 (AMD:26569-Rev.3.13-May.2013)
pfmul	PFMUL		page 107 (AMD:26569-Rev.3.13-May.2013)
pfnacc	PFNACC		page 109 (AMD:26569-Rev.3.13-May.2013)
pfpnacc	PFPNACC		page 112 (AMD:26569-Rev.3.13-May.2013)
pfrcp	PFRCP		page 115 (AMD:26569-Rev.3.13-May.2013)
pfrcpit1	PFRCPIT1		page 118 (AMD:26569-Rev.3.13-May.2013)
pfrcpit2	PFRCPIT2		page 121 (AMD:26569-Rev.3.13-May.2013)
pfersqit1	PFRSQIT1		page 124 (AMD:26569-Rev.3.13-May.2013)
pfersqrt	PFRSQRT		page 127 (AMD:26569-Rev.3.13-May.2013)
pfsub	PFSUB		page 130 (AMD:26569-Rev.3.13-May.2013)
pfsubr	PFSUBR		page 132 (AMD:26569-Rev.3.13-May.2013)
pi2fd	PI2FD		page 134 (AMD:26569-Rev.3.13-May.2013)

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
pi2fw	PI2FW		page 136 (AMD:26569-Rev.3.13-May.2013)
pmulhrw	PMULHRW		page 152 (AMD:26569-Rev.3.13-May.2013)
pswapd	PSWAPD		page 201 (AMD:26569-Rev.3.13-May.2013)

3.29 3DNowx Instructions

TABLE 3-69 3DNowx Instructions

Oracle Solaris Mnemonic	Intel/AMD Mnemonic	Description	Reference
prefetch	PREFETCH		page 256 (AMD:24594-Rev.3.20-May.2013)
prefetchw	PREFETCHW	prefetch data into Caches in anticipation of a write	page 10-9 (319433-016/Oct.2013)

3.30 64–Bit AMD Opteron Considerations

To assemble code for the AMD Opteron CPU, invoke the assembler with the `-m64` command line option. See the [as\(1\)](#) man page for additional information.

The following Oracle Solaris mnemonics are only valid when the `-m64` command line option is specified:

adcq	cmovnoq	mulq
addq	cmovnpq	negq
andq	cmovnsq	notq
bsfq	cmovnzq	orq
bsrq	cmovoq	popfq
bswapq	cmovpeq	popq
btcq	cmovpoq	pushfq
btq	cmovpq	pushq
btrq	cmovsq	rclq
btsq	cmovzq	rcrq
cltq	cmpq	rolq
cmovaeq	cmpsq	rorq

<code>cmovaq</code>	<code>cmpxchgq</code>	<code>salq</code>
<code>cmovbeq</code>	<code>cqtd</code>	<code>sarq</code>
<code>cmovbq</code>	<code>cqto</code>	<code>sbbq</code>
<code>cmovcq</code>	<code>decq</code>	<code>scasq</code>
<code>cmoveq</code>	<code>divq</code>	<code>shldq</code>
<code>cmovgeq</code>	<code>idivq</code>	<code>shlq</code>
<code>cmovgq</code>	<code>imulq</code>	<code>shrdq</code>
<code>cmovleq</code>	<code>incq</code>	<code>shrq</code>
<code>cmovlq</code>	<code>larq</code>	<code>sldtq</code>
<code>cmovnaeq</code>	<code>leaq</code>	<code>smswq</code>
<code>cmovnaq</code>	<code>lodsq</code>	<code>stosq</code>
<code>cmovnbeq</code>	<code>lslq</code>	<code>strq</code>
<code>cmovnbq</code>	<code>movabs</code>	<code>subq</code>
<code>cmovncq</code>	<code>movdq</code>	<code>testq</code>
<code>cmovneq</code>	<code>movntiq</code>	<code>xaddq</code>
<code>cmovngeq</code>	<code>movq</code>	<code>xchgq</code>
<code>cmovngq</code>	<code>movsq</code>	<code>xchgqA</code>
<code>cmovnlq</code>	<code>movswq</code>	<code>xorq</code>
<code>cmovnlq</code>	<code>movzsq</code>	

The following Oracle Solaris mnemonics are *not* valid when the `-m64` command line option is specified:

<code>aaa</code>	<code>daa</code>	<code>lesw</code>
<code>aad</code>	<code>das</code>	<code>popa</code>
<code>aam</code>	<code>into</code>	<code>popaw</code>
<code>aas</code>	<code>jecz</code>	<code>pusha</code>
<code>boundw</code>	<code>ldsw</code>	<code>pushaw</code>

◆◆◆ A P P E N D I X A

Using the Assembler Command Line

This appendix describes how to invoke the assembler from the command line, and details the command-line options.

A.1 Assembler Command Line

You invoke the assembler command line as follows:

```
as [options] [inputfile] ...
```

Note - The Oracle Solaris Studio C, C++, and Fortran compilers (`cc(1)`, `CC(1)`, and `f95(1)`) invoke the assembler with the `fbc` command. You can use either the `as` or `fbc` command on a Oracle Solaris platform to invoke the assembler. On an Oracle Solaris x86 platform, the `as` or `fbc` command will invoke the x86 assembler. On an Oracle Solaris SPARC platform, the command invokes the SPARC assembler.

The `as` command translates the assembly language source files, *inputfile*, into an executable object file, *objfile*. The assembler recognizes the filename argument *hyphen* (-) as the standard input. It accepts more than one file name on the command line. The input file is the concatenation of all the specified files. If an invalid option is given or the command line contains a syntax error, the assembler prints the error (including a synopsis of the command line syntax and options) to standard error output, and then terminates.

The assembler supports macros, `#include` files, and symbolic substitution through use of the C preprocessor `cpp(1)`. The assembler invokes the preprocessor before assembly begins if it has been specified from the command line as an option. (See the `-P` option.)

A.2 Assembler Command Line Options

-a32

Allow 32-bit addresses in 64-bit mode.

`-Dname -Dname=def`

When the `-P` option is in effect, these options are passed to the `cpp` preprocessor without interpretation by the `as` command; otherwise, they are ignored.

`-{n}H`

Enable (`-H`) or suppress (`-nH`) generation of the Hardware Capabilities section.

`-Ipath`

When the `-P` option is in effect, this option is passed to the `cpp` preprocessor without interpretation by the `as` command; otherwise, it is ignored.

`-i`

Ignore line number information from the preprocessor.

`-KPIC`

Check for address referencing with absolute relocation and issue warning.

`-m`

This option runs `m4` macro preprocessing on input. The `m4` preprocessor is more useful for complex preprocessing than the C preprocessor invoked by the `-P` option. See the `m4(1)` man page for more information about the `m4` macro-processor.

`-m64 | -m32`

Select the 64-bit (`-m64`) or 32-bit (`-m32`) memory model. With `-m64`, the resulting `.o` object files are in 64-bit ELF format and can only be linked with other object files in the same format. The resulting executable can only be run on a 64-bit x86 processor running 64-bit Oracle Solaris OS. `-m32` is the default.

`-n`

Suppress all warnings while assembling.

`-o outfile`

Write the output of the assembler to *outfile*. By default, if `-o` is not specified, the output file name is the same as the input file name with `.s` replaced with `.o`.

`-P`

Run `cpp(1)`, the C preprocessor, on the files being assembled. The preprocessor is run separately on each input file, not on their concatenation. The preprocessor output is passed to the assembler.

`-Q{y|n}`

This option produces the “assembler version” information in the comment section of the output object file if the `y` option is specified; if the `n` option is specified, the information is suppressed.

`-S[a|b|c|l|A|B|C|L]`

Produces a disassembly of the emitted code to the standard output. Adding each of the following characters to the `-S` option produces:

- `a` - disassembling with address
- `b` - disassembling with `".bof"`
- `c` - disassembling with comments
- `l` - disassembling with line numbers

Capital letters turn the switch off for the corresponding option.

`-s`

This option places all stabs in the `".stabs"` section. By default, stabs are placed in `".stabs.excl"` sections, which are stripped out by the static linker `ld` during final execution. When the `-s` option is used, stabs remain in the final executable because `".stab"` sections are not stripped out by the static linker `ld`.

`-Uname`

When the `-P` option is in effect, this option is passed to the `cpp` preprocessor without interpretation by the `as` command; otherwise, it is ignored.

`-V`

This option writes the version information on the standard error output.

`-xchip=processor`

processor specifies the target architecture processor. When there is a choice between several possible encodings, choose the one that is appropriate for the stated chip. In particular, use the appropriate no-op byte sequence to fill code alignment padding, and warn when instructions not defined for the stated chip are used.

The assembler accepts the instruction sets for the following recognized `-xchip` processor values:

<i>processor</i> value	Target Processor
generic	Generic x86
native	This host processor.
core2	Intel Core2
nehalem	Intel Nehalem
opteron	AMD Opteron
penryn	Intel Penryn
pentium	Intel Pentium
pentium_pro	Intel Pentium Pro
pentium3	Intel Pentium 3.
pentium4	Intel Pentium 4
sandybridge	Intel Sandy Bridge
westmere	Intel Westmere
amdfam10	AMD FAM10
ivybridge	Intel Ivy Bridge
haswell	Intel Hawell

`-xmodel=[small | medium | kernel]`

For `-m64` only, generate `R_X86_64_32S` relocatable type for data access under `kernel`. Otherwise, generate `R_X86_64_32` under `small`. `SHN_AMD64_LCOMMON` and `.lbcomm` support added under `medium`. The default is `small`.

`-Y{d|m},path`

Specify the path to locate the version of `cm4defs` (`-Yd,path`) or `m4` (`-Ym,path`) to use.

`-YI,path`

Indicate path to search for `#include` header files.

A.3 Disassembling Object Code

The `dis` program is the object code disassembler for ELF. It produces an assembly language listing of the object file. For detailed information about this function, see the `dis(1)` man page.

Index

Numbers and Symbols

.cfi_adjust_cfa_offset OFFSET, 21
.cfi_def_cfa REGISTER, OFFSET, 21
.cfi_def_cfa_offset OFFSET, 21
.cfi_def_cfa_register REGISTER, 21
.cfi_endproc, 21
.cfi_escape EXPRESSION[, ...], 21
.cfi_offset REGISTER, OFFSET, 21
.cfi_rel_offset REGISTER, OFFSET, 22
.cfi_startproc, 22

A

-a32 option, 123
aaa, 33
aad, 33
aam, 33
aas, 34
adc, 33
add, 33
addpd, 104
addps, 97
addressing, 19
addsd, 104
addss, 97
addsubpd, 111
addsubps, 111
aesdec, 48
aesdeclast, 48
aesenc, 48
aesenclast, 49
aesimc, 49
aeskeygenassist, 49
.align, 20

and, 34
andn, 82
andnpd, 105
andnps, 99
andpd, 105
andps, 99
arpl, 117
as
 syntax, UNIX versus Intel, 11
as command, 123
.ascii, 20
assembler command line, 123
assembler command line options, 123

B

.bcd, 20
bextr, 82
binary arithmetic instructions, 33
bit instructions, 35
blendpd, 112
blendps, 112
blendvpd, 112
blendvps, 112
blsi, 82
blmsk, 82
blsr, 82
bound, 37
bsf, 35
bsr, 35
.bss, 20
bswap, 29
bt, 35
btc, 35

btr, 35
bts, 35
.2byte, 20
.4byte, 20
.8byte, 20
.byte, 20
byte instructions, 35
bzhi, 82

C

call, 37
cbtw, 29
clc, 41
cld, 41
clflush, 110
cli, 41
cltd, 30
cltq, 30
clts, 117
cmc, 41
cmova, 30
cmov.a, 30
cmovae, 30
cmov.ae, 30
cmovb, 30
cmov.b, 30
cmovbe, 30
cmov.be, 30
cmovc, 30
cmov.c, 30
cmove, 30
cmov.e, 30
cmovg, 30
cmov.g, 30
cmovge, 30
cmov.ge, 30
cmovl, 30
cmov.l, 30
cmovle, 30
cmov.le, 30
cmovna, 30
cmov.na, 30
cmovnae, 30
cmov.nae, 30
cmovnb, 30
cmov.nb, 30
cmovnbe, 30
cmov.nbe, 30
cmovnc, 30
cmov.nc, 30
cmovne, 30
cmov.ne, 30
cmovng, 31
cmov.ng, 31
cmovnge, 31
cmov.nge, 31
cmovnl, 31
cmov.nl, 31
cmovnle, 31
cmov.nle, 31
cmovno, 31
cmov.no, 31
cmovnp, 31
cmov.np, 31
cmovns, 31
cmov.ns, 31
cmovnz, 31
cmov.nz, 31
cmovo, 31
cmov.o, 31
cmovp, 31
cmov.p, 31
cmovpe, 31
cmovpo, 31
cmovs, 31
cmovz, 31
cmp, 33
cmppd, 106
cmpps, 99
cmps, 39
cmpsb, 39
cmpsd, 106
cmpsl, 39

cmpss, 99
cmpsw, 39
cmpxchg, 31
cmpxchg8b, 31
comisd, 106
comiss, 99
.comm, 22
command-line options, 123
comment, 13
compiler drivers, 123
control transfer instructions, 36
cpuid, 42
cqtd, 31
cqto, 31
cvtdq2pd, 107
cvtdq2ps, 109
cvtpd2dq, 107
cvtpd2pi, 107
cvtpd2ps, 107
cvtpi2pd, 107
cvtpi2ps, 100
cvtps2dq, 109
cvtps2pd, 108
cvtps2pi, 100
cvtsd2si, 108
cvtsd2ss, 108
cvtsi2sd, 108
cvtsi2ss, 100
cvtss2sd, 108
cvtss2si, 100
cvttpd2dq, 108
cvttpd2pi, 108
cvttps2dq, 109
cvttps2pi, 101
cvttsd2si, 108
cvtss2si, 101
cwtd, 32
cwtl, 32

D

-D option, 124
daa, 34

das, 34
.data, 23
data transfer instructions, 29
dec, 33
decimal arithmetic instructions, 33
directives, 20
dis program, 127
disassembling object code, 127
div, 33
divpd, 104
divps, 97
divsd, 104
divss, 97
.double, 23
dppd, 112
dpps, 112

E

emms, 94
enter, 37
.even, 23
.ext, 23
extensions
 transactional synchronization, 116
extractps, 112
extrq, 112

F

f2xm1, 45
fabs, 43
fadd, 43
faddp, 43
fbc command, 123
fbld, 42
fbstp, 42
fchs, 43
fclex, 46
fcmovb, 42
fcmovbe, 42
fcmovs, 42
fcmovnb, 43

fcmovnbe, 43
fcmovne, 43
fcmovnu, 43
fcmovu, 43
fcom, 45
fcomi, 45
fcomip, 45
fcomp, 45
fcompp, 45
fcos, 46
fdecstp, 47
fdiv, 43
fdivp, 43
fdivr, 44
fdivrp, 44
femms, 119
ffree, 47
fiadd, 44
ficom, 45
ficomp, 45
fidiv, 44
fidivr, 44
fild, 43
.file, 23
fimul, 44
fincstp, 47
finit, 47
fist, 43
fistp, 43
fisub, 44
fisubr, 44
flag control instructions, 40
fld, 43
fld1, 46
fldcw, 47
fldenv, 47
fldl2e, 46
fldl2t, 46
fldlg2, 46
fldln2, 46
fldpi, 46
fldz, 46
.float, 23
floating-point instructions
 basic arithmetic, 43
 comparison, 44
 control, 46
 data transfer, 42
 load constants, 46
 logarithmic *See* transcendental
 transcendental, 45
 trigonometric *See* transcendental
fmul, 44
fmulp, 44
fnclex, 47
fninit, 47
fnop, 47
fnsave, 47
fnstcw, 47
fnstenv, 47
fnstsw, 47
fpatan, 46
fprem, 44
fprem1, 44
fptan, 46
frndint, 44
frstor, 47
fsave, 47
fscale, 44
fsin, 46
fsincos, 46
fsqrt, 44
fst, 43
fstcw, 48
fstenv, 48
fstp, 43
fstsw, 48
fsub, 44
fsubp, 44
fsubr, 44
fsubrp, 44
ftst, 45
fucom, 45
fucomi, 45
fucomip, 45

fucomp, 45
 fucompp, 45
 fwait, 48
 fxam, 45
 fxch, 43
 fxrstor, 48
 fxsave, 48
 fxtract, 44
 fyl2x, 46
 fyl2xp1, 46

G

gas, 11
 .globl, 23
 .group, 23

H

-{n}H option, 124
 haddpd, 111
 haddps, 111
 .hidden, 23
 hlt, 117
 hsubpd, 111
 hsubps, 111
 hyphen (-), 123

I

-I option, 124
 -i option, 124
 I/O (input/output) instructions, 40
 .ident, 23
 identifier, 15
 idiv, 33
 imul, 33
 in, 40
 inc, 33
 ins, 40
 insb, 40
 insertps, 113
 insertq, 112

insl, 40
 instruction, 17
 format, 17
 suffixes, 18
 instructions
 3DNow, 119
 3DNowx, 121
 Advanced Vector Extensions, 49
 AES, 48
 AVX, 49
 AVX2, 74
 binary arithmetic, 33
 bit, 35
 BMI1, 82
 BMI2, 82
 byte, 35
 control transfer, 36
 data transfer, 29
 decimal arithmetic, 33
 F16C, 83
 flag control, 40
 floating-point, 42
 FMA, 83
 FSGSBASE, 90
 I/O (input/output), 40
 logical, 34
 miscellaneous, 42
 MMX, 90
 MOVBE, 95
 operating system support, 117
 Opteron, 121
 PCLMULQDQ, 95
 RDRAND, 95
 rotate, 34
 segment register, 41
 shift, 34
 SIMD state management, 48
 SSE, 95
 SSE2, 103
 SSE3, 111
 SSE4.1, 112
 SSE4.2, 115
 SSE4a, 112
 SSSE3, 115
 string, 38
 VMX, 118

XSAVE, 119
insw, 40
int, 37
into, 37
invd, 117
invept, 118
invlpg, 117
invoking, as command, 123
invpcid, 32
invvpid, 118
iret, 37

J

ja, 37
jae, 37
jb, 37
jbe, 37
jc, 37
jcxz, 37
je, 37
jecxz, 37
jg, 37
jge, 37
jl, 37
jle, 37
jmp, 37
jnae, 37
jnb, 37
jnbe, 37
jnc, 37
jne, 37
jng, 37
jnge, 37
jnl, 37
jnle, 38
jno, 38
jnp, 38
jns, 38
jnz, 38
jo, 38
jp, 38
jpe, 38

jpo, 38
js, 38
jz, 38

K

keyword, 15
-KPIC option, 124

L

label, 14
 numeric, 14
 symbolic, 14
lahf, 41
lar, 117
lcall, 38
lcomm, 24
lddqu, 111
ldmxcsr, 101
lds, 41
lea, 42
leave, 38
les, 41
lfence, 110
lfs, 41
lgdt, 117
lgs, 41
lidt, 117
lldt, 117
lmsw, 117
.local, 24
lock, 117
lods, 39
lodsb, 39
lodsl, 39
lodsw, 39
logical instructions, 34
.long, 24
loop, 38
loope, 38
loopne, 38
loopnz, 38

loopz, 38
 lret, 38
 lsl, 117
 lss, 41
 ltr, 117
 lzcnt(|q|l|w), 82

M

-m option, 124
 -m64 and -m32 options, 124
 maskmovdqu, 110
 maskmovq, 102
 maxpd, 104
 maxps, 97
 maxsd, 105
 maxss, 97
 mfence, 110
 minpd, 105
 minps, 97
 minsd, 105
 minss, 98
 miscellaneous instructions, 42
 MMX instructions
 comparison, 93
 conversion, 91
 data transfer, 90
 logical, 93
 packed arithmetic, 91
 rotate, 94
 shift, 94
 state management, 94
 mov, 32
 movabs, 32
 movabsA, 32
 movapd, 103
 movaps, 96
 movbe(|q|l|w), 95
 movd, 91
 movddup, 111
 movdq2q, 109
 movdqa, 109
 movdqu, 109
 movhlps, 96
 movhpd, 103
 movhps, 96
 movlhps, 96
 movlpd, 104
 movlps, 96
 movmskpd, 104
 movmskps, 97
 movntdq, 110
 movntdqa, 113
 movnti, 110
 movntpd, 110
 movntps, 102
 movntq, 102
 movntsd, 112
 movntss, 112
 movq, 91
 movq2dq, 109
 movs, 39
 movsb, 32, 39
 movsd, 104
 movshdup, 111
 movsl, 39
 movsldup, 111
 movss, 97
 movsw, 32, 39
 movupd, 104
 movups, 97
 movzb, 32
 movzw, 32
 mpsadbw, 113
 mul, 33
 mulpd, 105
 mulps, 98
 mulsd, 105
 mulss, 98
 multiple files, on, 123
 mulx, 82

N

-n option, 124
 neg, 33

- nop, 42
- not, 34
- numbers, 15
 - floating point, 16
 - integers, 15
 - binary, 15
 - decimal, 15
 - hexadecimal, 15
 - octal, 15

O

- o option, 124
- operands, 18
 - immediate, 19
 - indirect, 18
 - memory
 - addressing, 19
 - ordering (source, destination), 18
 - register, 19
- operating system support instructions, 117
- Opteron instructions, 121
- options
 - command-line, 123
- or, 34
- orpd, 106
- orps, 99
- out, 40
- outs, 40
- outsb, 40
- outsl, 40
- outsw, 40

P

- P option, 125
- pabs(w|b|d), 115
- packssdw, 91
- packsswb, 91
- packusdw, 113
- packuswb, 91
- paddb, 92
- paddd, 92
- paddq, 109

- paddsb, 92
- paddsw, 92
- paddusb, 92
- paddusw, 92
- paddw, 92
- palignr, 115
- pand, 93
- pandn, 93
- pause, 111
- pavgb, 101
- pavgusb, 119
- pavgw, 101
- pblendvb, 113
- pblendw, 113
- pclmulqdq, 95
- pcmpeqb, 93
- pcmpeqd, 93
- pcmpeqq, 113
- pcmpeqw, 93
- pcmpetri, 115
- pcmpetrm, 115
- pcmpgtb, 93
- pcmpgtd, 93
- pcmpgtq, 115
- pcmpgtw, 93
- pcmpistri, 115
- pcmpistrm, 115
- pdep, 82
- pext, 82
- pextr(q|b|d), 113
- pextrw, 101, 113
- pf2id, 119
- pf2iw, 120
- pfacc, 120
- pfadd, 120
- pfcmpeq, 120
- pfcmpge, 120
- pfcmpgt, 120
- pfmax, 120
- pfmin, 120
- pfmul, 120
- pfnacc, 120

pfpnacc, 120
pfrcp, 120
pfrcpit1, 120
pfrcpit2, 120
pfrsqit1, 120
pfrsqr, 120
pfsb, 120
pfsbr, 120
phadd(w|d), 115
phaddsw, 115
phminposuw, 113
phsub(w|d), 116
phsubsw, 116
pi2fd, 120
pi2fw, 121
pinsr(q|b|d), 113
pinsrw, 101
pmaddubsw, 116
pmaddwd, 92
pmaxs(b|d), 113
pmaxsw, 101
pmaxub, 102
pmaxud, 113
pmaxuw, 114
pminsb, 114
pminsd, 114
pminsw, 102
pminub, 102
pminud, 114
pminuw, 114
pmovmskb, 102
pmovsx(bd|bq|bw|dq|wd|wq), 114
pmovzx(bd|bq|bw|dq|wd|wq), 114
pmuldq, 114
pmulhrsw, 116
pmulhrw, 121
pmulhw, 102
pmulhw, 92
pmulld, 114
pmullw, 92
pmuludq, 109
pop, 32
popa, 32
popal, 32
popaw, 32
popf, 41
popfw, 41
.popsection, 24
por, 93
prefetch, 121
prefetchnta, 102
prefetcht0, 102
prefetcht1, 103
prefetcht2, 103
prefetchw, 121
.previous, 24
psadbw, 102
pshufb, 116
pshufd, 109
pshufhw, 109
pshuflw, 109
pshufw, 102
psign(w|b|d), 116
pslld, 94
pslldq, 110
psllq, 94
psllw, 94
psrad, 94
psraw, 94
psrld, 94
psrldq, 110
psrlq, 94
psrlw, 94
psubb, 92
psubd, 92
psubq, 110
psubsb, 92
psubsw, 92
psubusb, 92
psubusw, 92
psubw, 93
pswapd, 121
ptest, 114
punpckhbw, 91

punpckhdq, 91
punpckhqdq, 110
punpckhwd, 91
punpcklbw, 91
punpckldq, 91
punpcklqdq, 110
punpcklwd, 91
push, 32
pusha, 32
pushal, 32
pushaw, 32
pushf, 41
pushfw, 41
.pushsection, 24
pxor, 93

Q

-Q option, 125
.quad, 24

R

rcl, 34
rcpps, 98
rcpss, 98
rcr, 34
rdfsbase(|l|q), 90
rdgsbase(|l|q), 90
rdmsr, 117
rdpmc, 117
rdrand(|q|l|w), 95
rdtsc, 117
.rel, 24
rep, 39
repnz, 39
repz, 39
ret, 38
rol, 34
ror, 34
rorx, 82
rotate instructions, 34
roundpd, 114

roundps, 114
roundsd, 114
roundss, 114
rsm, 117
rsqrtps, 98
rsqrtss, 98

S

-S option, 125
-s option, 125
sahf, 41
sal, 34
sar, 34
sarx, 82
sbb, 33
scas, 39
scasb, 39
scasl, 39
scasw, 40
.section, 24
segment register instructions, 41
.set, 25
seta, 35
setae, 35
setb, 35
setbe, 35
setc, 35
sete, 35
setg, 35
setge, 35
setl, 35
setle, 35
setna, 35
setnae, 36
setnb, 36
setnbe, 36
setnc, 36
setne, 36
setng, 36
setnge, 36
setnl, 36
setnle, 36

-
- setno, 36
 - setnp, 36
 - setns, 36
 - setnz, 36
 - seto, 36
 - setp, 36
 - setpe, 36
 - setpo, 36
 - sets, 36
 - setz, 36
 - sfence, 103
 - sgdt, 117
 - shift instructions, 34
 - shl, 34
 - shld, 35
 - shlx, 83
 - shr, 35
 - shrd, 35
 - shrx, 83
 - shufpd, 107
 - shufps, 100
 - sidt, 117
 - SIMD state management instructions, 48
 - .size, 25
 - .skip, 25
 - sldt, 118
 - .sleb128, 25
 - smovl, 39
 - smsw, 118
 - sqrtpd, 105
 - sqrtps, 98
 - sqrtsd, 105
 - sqrtss, 98
 - SSE instructions
 - compare, 98
 - conversion, 100
 - data transfer, 96
 - integer (64-bit SIMD), 101
 - logical, 99
 - miscellaneous, 102
 - MXCSR state management, 101
 - packed arithmetic, 97
 - shuffle, 100
 - unpack, 100
 - SSE2 instructions
 - compare, 106
 - conversion, 107
 - data movement, 103
 - logical, 105
 - miscellaneous, 110
 - packed arithmetic, 104
 - packed single-precision floating-point, 108
 - shuffle, 106
 - SIMD integer instructions (128-bit), 109
 - unpack, 106
 - statement, 13
 - empty, 13
 - stc, 41
 - std, 41
 - sti, 41
 - stmxcsr, 101
 - stos, 40
 - stosb, 40
 - stosl, 40
 - stosw, 40
 - str, 118
 - string, 16
 - .string, 25
 - string instructions, 38
 - sub, 33
 - subpd, 105
 - subps, 98
 - subsd, 105
 - subss, 98
 - .symbolic, 25
 - sysenter, 118
 - sysexit, 118
- T**
- .tbss, 25
 - .tcomm, 25
 - .tdata, 25
 - test, 36
 - .text, 25
 - .type, 25
 - tzcnt, 82

U

-U option, 125
ucomisd, 106
ucomiss, 99
ud2, 42
.uleb128, 25
unpckhpd, 107
unpckhps, 100
unpcklpd, 107
unpcklps, 100

V

-V option, 125
vaddpd, 49
vaddps, 49
vaddsd, 50
vaddss, 50
vaddsubpd, 50
vaddsubps, 50
vaesdec, 49
vaesdeclast, 49
vaesenc, 49
vaesenclast, 49
vaesimc, 49
vaeskeygenassist, 49
.value, 26
vandnpd, 50
vandnps, 50
vandpd, 50
vandps, 50
vblendpd, 50
vblendps, 50
vblendvpd, 50
vblendvps, 50
vbroadcast(f128|sd|ss), 73
vbroadcast(sd|ss), 80
vbroadcasti128, 80
vcmpcq_ospd, 50
vcmpcq_osps, 53
vcmpcq_ossd, 55
vcmpcq_oss, 57
vcmpcq_uqpd, 50
vcmpcq_uqps, 53
vcmpcq_uqsd, 55
vcmpcq_uqss, 58
vcmpcq_uspd, 51
vcmpcq_usps, 53
vcmpcq_ussd, 55
vcmpcq_uss, 58
vcmpcqpdp, 51
vcmpcqpdp, 53
vcmpcqpdp, 55
vcmpcqpdp, 58
vcmpfalse_ospd, 51
vcmpfalse_osps, 53
vcmpfalse_ossd, 55
vcmpfalse_oss, 58
vcmpfalsepd, 51
vcmpfalseps, 53
vcmpfalsepd, 55
vcmpfalseps, 58
vcmpge_oqpd, 51
vcmpge_oqps, 53
vcmpge_oqsd, 56
vcmpge_oqss, 58
vcmpgepd, 51
vcmpgeps, 53
vcmpgesd, 56
vcmpgess, 58
vcmpgt_oqpd, 51
vcmpgt_oqps, 53
vcmpgt_oqsd, 56
vcmpgt_oqss, 58
vcmpgtpd, 51
vcmpgtps, 53
vcmpgtsd, 56
vcmpgtss, 58
vcmppl_oqpd, 51
vcmppl_oqps, 53
vcmppl_oqsd, 56
vcmppl_oqss, 58
vcmpplpd, 51
vcmpplps, 54
vcmpplsd, 56

vcmpless, 58
vcmplt_oqpd, 51
vcmplt_oqps, 54
vcmplt_oqsd, 56
vcmplt_oqss, 58
vcmpltpd, 51
vcmpltps, 54
vcmpltsd, 56
vcmpltss, 58
vcmpneq_oqpd, 51
vcmpneq_oqps, 54
vcmpneq_oqsd, 56
vcmpneq_oqss, 58
vcmpneq_ospd, 51
vcmpneq_osps, 54
vcmpneq_ossd, 56
vcmpneq_osss, 59
vcmpneq_uspd, 52
vcmpneq_usps, 54
vcmpneq_ussd, 56
vcmpneq_usss, 59
vcmpneqpd, 52
vcmpneqps, 54
vcmpneqsd, 56
vcmpneqss, 59
vcmpnge_uqpd, 52
vcmpnge_uqps, 54
vcmpnge_uqsd, 56
vcmpnge_uqss, 59
vcmpngepd, 52
vcmpngeps, 54
vcmpngesd, 56
vcmpngess, 59
vcmpngt_uqpd, 52
vcmpngt_uqps, 54
vcmpngt_uqsd, 57
vcmpngt_uqss, 59
vcmpngtpd, 52
vcmpngtps, 54
vcmpngtsd, 57
vcmpngtss, 59
vcmpnle_uqpd, 52
vcmpnle_uqps, 54
vcmpnle_uqsd, 57
vcmpnle_uqss, 59
vcmpnlepd, 52
vcmpnleps, 54
vcmpnlesd, 57
vcmpnless, 59
vcmpnlt_uqpd, 52
vcmpnlt_uqps, 54
vcmpnlt_uqsd, 57
vcmpnlt_uqss, 59
vcmpnltpd, 52
vcmpnltps, 55
vcmpnltsd, 57
vcmpnlts, 59
vcmpord_spd, 52
vcmpord_sps, 55
vcmpord_ssd, 57
vcmpord_sss, 59
vcmpordpd, 52
vcmpordps, 55
vcmpordsd, 57
vcmpordss, 59
vcmpdpd, 52
vcmppps, 55
vcmpsd, 57
vcmpss, 59
vcmptrue_uspd, 52
vcmptrue_usps, 55
vcmptrue_ussd, 57
vcmptrue_usss, 60
vcmptruepd, 53
vcmptrueps, 55
vcmptruesd, 57
vcmptruess, 60
vcmpunord_spd, 53
vcmpunord_sps, 55
vcmpunord_ssd, 57
vcmpunord_sss, 60
vcmpunordpd, 53
vcmpunordps, 55
vcmpunordsd, 57

vcmpunordss, 60
vcomisd, 60
vcomiss, 60
vcvtdq2pd, 60
vcvtdq2ps, 60
vcvtpd2dq(|x|y), 60
vcvtpd2ps(|x|y), 60
vcvtph2ps, 83
vcvtps2dq, 60
vcvtps2pd, 60
vcvtps2ph, 83
vcvtss2si(|q|l), 61
vcvtss2ss, 61
vcvtss2sd(|q|l), 61
vcvtss2ss(|q|l), 61
vcvtss2sd, 61
vcvtss2si(|q|l), 61
vcvtss2sd(|x|y), 61
vcvtss2sd, 61
vcvtss2si(|q|l), 61
vcvtss2ss(|q|l), 61
vdivpd, 62
vdivps, 62
vdivsd, 62
vdivss, 62
vdppd, 62
vdpps, 62
verr, 118
verw, 118
vextractf128, 73
vextracti128, 80
vextractps, 62
vmadd132pd, 83
vmadd132ps, 84
vmadd132sd, 84
vmadd132ss, 84
vmadd213pd, 83
vmadd213ps, 84
vmadd213sd, 84
vmadd213ss, 84
vmadd231pd, 84
vmadd231ps, 84
vmadd231sd, 84
vmadd231ss, 84
vmaddsub132pd, 85
vmaddsub132ps, 85
vmaddsub213pd, 85
vmaddsub213ps, 85
vmaddsub231pd, 85
vmaddsub231ps, 85
vmfsub132pd, 85
vmfsub132ps, 86
vmfsub132sd, 86
vmfsub132ss, 86
vmfsub213pd, 85
vmfsub213ps, 86
vmfsub213sd, 86
vmfsub213ss, 86
vmfsub231pd, 85
vmfsub231ps, 86
vmfsub231sd, 86
vmfsub231ss, 86
vmfsubadd132pd, 86
vmfsubadd132ps, 87
vmfsubadd213pd, 87
vmfsubadd213ps, 87
vmfsubadd231pd, 87
vmfsubadd231ps, 87
vmfmadd132pd, 87
vmfmadd132ps, 87
vmfmadd132sd, 88
vmfmadd132ss, 88
vmfmadd213pd, 87
vmfmadd213ps, 88
vmfmadd213sd, 88
vmfmadd213ss, 88
vmfmadd231pd, 87
vmfmadd231ps, 88
vmfmadd231sd, 88
vmfmadd231ss, 88
vmfnmsub132pd, 88
vmfnmsub132ps, 89
vmfnmsub132sd, 89
vmfnmsub132ss, 89

vfnmsub213pd, 88
vfnmsub213ps, 89
vfnmsub213sd, 89
vfnmsub213ss, 89
vfnmsub231pd, 89
vfnmsub231ps, 89
vfnmsub231sd, 89
vfnmsub231ss, 90
vgatherdp(d|s), 80
vgatherqp(d|s), 80
vhaddpd, 62
vhaddps, 62
vhsubpd, 62
vhsubps, 62
vinsertf128, 73
vinserti128, 80
vinsertps, 62
vladdqu, 62
vlmaskcsr, 62
vmaskmov(pd|ps), 73
vmaskmovdqu, 63
vmaxpd, 63
vmaxps, 63
vmaxsd, 63
vmaxss, 63
vmcall, 118
vmclear, 118
vmfunc, 118
vminpd, 63
vminps, 63
vminsd, 63
vminss, 63
vmlaunch, 118
vmov(q|d), 63
vmovapd, 63
vmovaps, 63
vmovddup, 63
vmovdqa, 63
vmovdqu, 64
vmovhlps, 64
vmovhpd, 64
vmovhps, 64
vmovlhps, 64
vmovlpd, 64
vmovlps, 64
vmovmskpd, 64
vmovmskps, 64
vmovntdq, 64
vmovntdqa, 64, 74
vmovntpd, 64
vmovntps, 64
vmovq, 65
vmovsd, 65
vmovshdup, 65
vmovsldup, 65
vmovss, 65
vmovupd, 65
vmovups, 65
vmopsadbw, 65, 74
vmptrlld, 119
vmptrst, 119
vmread, 119
vmresume, 119
vmulpd, 65
vmulps, 65
vmulsd, 65
vmulss, 65
vmwrite, 119
vmxoff, 119
vmxon, 119
vorpd, 65
vorps, 65
vpabs(w|b|d), 66, 74
vpackss(dw|wb), 66, 75
vpackusdw, 66, 75
vpackuswb, 66, 75
vpadd(q|w|b|d), 66, 75
vpadds(w|b), 66, 75
vpaddus(w|b), 66, 75
vpalignr, 66, 75
vpand, 66, 75
vpandn, 66, 75
vpavg(w|b), 66, 75
vpblendd, 80

vpblendvb, 66, 75
vpblendw, 67, 75
vpbroadcast(q|w|b|d), 80
vpclmulqdq, 74
vpcmpeq(q|w|b|d), 67, 76
vpcmpestri, 67
vpcmpestrm, 67
vpcmpgt(q|w|b|d), 67, 76
vpcmpistri, 67
vpcmpistrm, 67
vperm2f128, 73
vperm2i128, 80
vpermd, 80
vpermilpd, 73
vpermilps, 73
vpermpd, 80
vpermps, 80
vpermq, 81
vpextr(q|b|d), 67
vpextrw, 67
vpgatherdd, 81
vpgatherdq, 81
vpgatherqd, 81
vpgatherqq, 81
vphadd(w|d), 67, 76
vphaddsw, 67, 76
vphminposuw, 67
vphsub(w|d), 68, 76
vphsubsw, 68, 76
vpinsr(q|b|w|d), 68
vpinsrw, 68
vpmaddubsw, 68, 76
vpmaddwd, 68, 76
vpmaskmov(q|d), 81
vpmxs(w|b|d), 68, 76
vpmxub, 68, 76
vpmxud, 68, 76
vpmxuw, 68, 77
vpminsb, 68, 77
vpminsd, 68, 77
vpminsw, 68, 77
vminub, 69, 77
vminud, 69, 77
vminuw, 69, 77
vpmovmskb, 69, 77
vpmovsx(bd|bq|bw|dq|wd|wq), 69, 77
vpmovzx(bd|bq|bw|dq|wd|wq), 69, 77
vpmuldq, 69, 77
vpmulhrsw, 69, 77
vpmulhuw, 69, 77
vpmulhw, 69, 77
vpmulld, 69, 78
vpmullw, 69, 78
vpmuludq, 69, 78
vpor, 69, 78
vpsadbw, 70, 78
vpsshufb, 70, 78
vpsshufd, 70, 78
vpsshufhw, 70, 78
vpsshufw, 70, 78
vpsign(w|b|d), 70, 78
vpsll(q|w|d), 70, 78
vpslldq, 70, 78
vpsllv(q|d), 81
vpsra(w|d), 70, 79
vpsravd, 81
vpsrl(q|w|d), 70, 79
vpsrldq, 70, 79
vpsrlv(q|d), 81
vpsub(q|w|b|d), 70, 79
vpsubs(w|b), 71, 79
vpsubus(w|b), 71, 79
vptest, 71
vpunpckh(bw|dq|qdq|wd), 71, 79
vpunpckl(bw|dq|qdq|wd), 71, 79
vpxor, 71, 79
vrcpps, 71
vrcpss, 71
vroundpd, 71
vroundps, 71
vroundsd, 71
vroundss, 71
vrsqrtps, 72
vrsqrtss, 72

vshufpd, 72
vshufps, 72
vsqrtpd, 72
vsqrtps, 72
vsqrtsd, 72
vsqrtss, 72
vstmxcsr, 72
vsubpd, 72
vsubps, 72
vsubsd, 72
vsubss, 72
vtestp(d|s), 74
vucomisd, 72
vucomiss, 73
vunpckhpd, 73
vunpckhps, 73
vunpcklpd, 73
vunpcklps, 73
vxorpd, 74
vxorps, 74
vzeroall, 74
vzeroupper, 74

W

wait, 48
wbinvd, 118
.weak, 26
whitespace, 13
wrfsbase(|l|q), 90
wrgsbases(|l|q), 90
wrmsr, 118

X

xabort, 116
xadd, 32
xbegin(|l|w), 116
xchg, 32
xchgA, 32
-xchip option, 125
xend, 116

xlat, 42
xlatb, 42
-xmodel option, 126
xor, 34
xorpd, 106
xorps, 99
xsaveopt(64|), 119
xtest, 116, 116

Y

-Y{d|m} option, 126
-YI option, 126

Z

.zero, 26

